CMR INSTITUTE OF TECHNOLOGY

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Internal Assesment Test - III

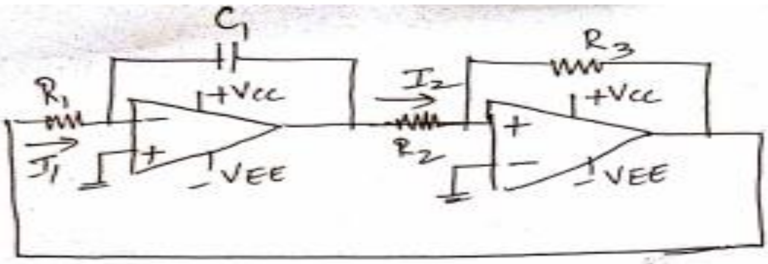
Sub:	**OPERATIONAL AMPLIFIERS AND LINEAR ICs**							Code:	15EE46
Date:	22/05/2018	Duration:	90 mins	Max Marks:	50	Sem :	**4th A**	Branch:	EEE

Answer Any FIVE FULL Questions

		Marks	OBE CO	OBE RBT
1a	Design a triangular waveform generator to produce ±2 V, 1kHz output. Use ±15V supply and explain the operation with help of waveforms.	10	CO5	L3
	OR			
1b	Explain the circuit of a full wave precision rectifier using half wave rectifier and summing circuit. Demonstrate the input and output waveforms.	10	CO3	L2
2a	Design a Inverting Schmitt trigger to have UTP=+2V and LTP=-3V using uA741 Op-amp with supply voltage Vcc=±15V.	10	CO4	L3
	OR			
2b	Explain the working of a 4 bit R-2R ladder type DAC.An 8 bit DAC has resolution of 20mV/LSB.Find V_{oFS} and V_o if the input is $(10000000)_2$.	10	CO2	L3
3a	Demonstrate the working of a non inverting comparator with positive and negative reference voltage and voltage to current converter with floating load.	10	CO4	L2
	OR			
3b	Explain the working of successive approximation ADC and dual slope ADC with block diagram	10	CO2	L2
4	Explain the operation of PLL with help of block diagram. Explain each block in detail.	10	CO6	L2
5	Sketch the internal circuit diagram of 555 monostable multivibrator .Draw the required waveforms and explain its operation	10	CO6	L2
6	Design a astable multivibrator using 555 timer for a frequency of 1kHz and duty cycle of 70%.Use C=0.1uF.Discuss any two applications of IC555.	10	CO6	L3

Solution

1a.



$$R_1 = \frac{V_{sat}}{I_1} = \frac{14}{100\mu A} = \frac{14}{100\times10^{-6}} \quad \frac{14}{10^{-4}}$$

$$\simeq 140\,k\Omega \; (120\,k\Omega)$$

$$R_3 = R_1 = 120\,k\Omega$$

$$R_2 = \frac{UTP}{I_1} = \frac{2}{100\mu A} = \frac{2}{10^{-4}} = 20\,k\Omega \simeq 18\,k\Omega$$

$$Q = CV \qquad C = \frac{Q}{V} = \frac{I_1 t}{\Delta V}$$

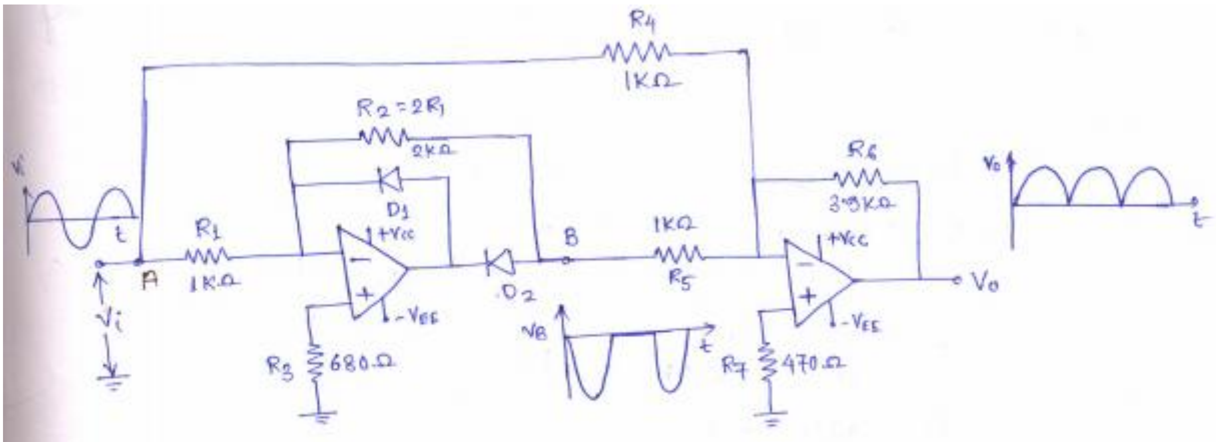
$$t = \frac{1}{2f} = \frac{1}{2\times10^3} = 500\mu s = 0.5\times10^{-3}$$

$$= \frac{100\times10^{-6}\times500\times10^{-6}}{4} = 12500\times10^{-12}$$

$$0.12500\times10^{-7}$$

$$= 0.01\,\mu F$$

1b.



The above circuit is a combination of half-wave rectifier with gain = 2 and an inverting adder with gain = 3.9

The above circuit is a combination of half-wave rectifier with gain = 2 and an inverting adder with gain = 39

During +ve half-cycle

Voltage at terminal A = $+V_i$

while that at terminal B is $-2V_i$.

[Diode D_1 is off and D_2 is on]

The output of the summing circuit, with $R_4 = R_5$

$$V_0 = -\frac{R_6}{R_4}(V_A + V_B)$$

$$= -\frac{R_6}{R_4}(V_i - 2V_i)$$

$$= -\frac{R_6}{R_4}(-V_i) = \frac{R_6}{R_4}V_i$$

During -ve half-cycle

$V_A = -V_i$

$V_B = 0$ as D_1 is on and D_2 is off.

consequently the output is,

$$V_0 = -\frac{R_6}{R_4}(V_A + V_B) = -\frac{R_6}{R_4}(-V_i + 0)$$

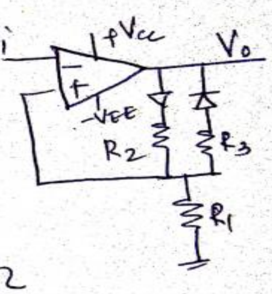
$$\boxed{V_0 = +\frac{R_6}{R_4}V_i}$$

2a.

UTP = +2

LTP = −3

$$R_1 = \frac{UTP}{I_1} = \frac{+2}{500\mu A} = 4k\Omega (3.9k\Omega)$$



$$UTP = \frac{(V_0 - V_D)R_1}{R_1 + R_2} \Rightarrow R_2 = \underline{\underline{22k\Omega}}$$

$$LTP = \frac{(V_0 - V_D) \times R_1}{R_1 + R_3} \Rightarrow R_3 = 15k\Omega$$

2b.

R-2R Ladder DAC

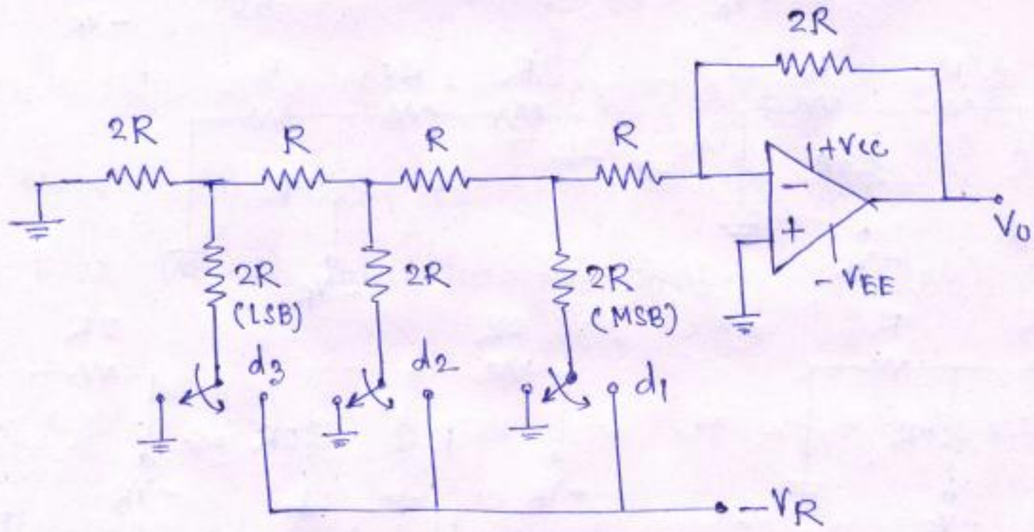


Fig- R-2R Ladder type DAC

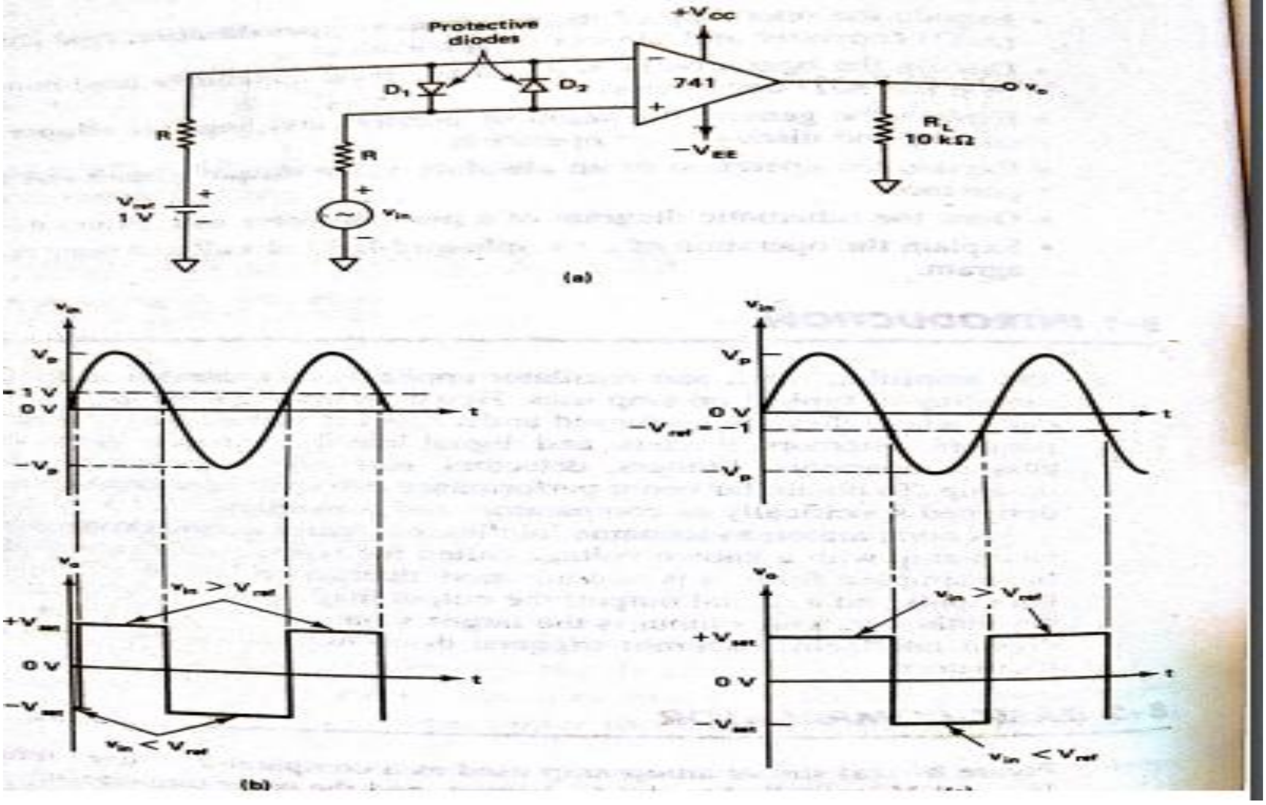
The range for R is 2.5 KΩ to 10 KΩ.

For simplicity, consider a 3-bit DAC. where $d_1 d_2 d_3$ corresponds to the binary word input to the DAC.

$-V_R$ is the reference voltage.

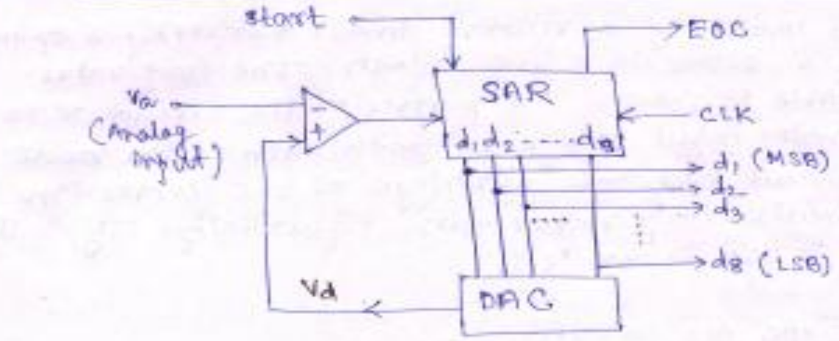
The feedback resistance is 2R. The network consist of R-2R network connected with the op-amp.

3a



3b

Successive Approximation type A/D converter

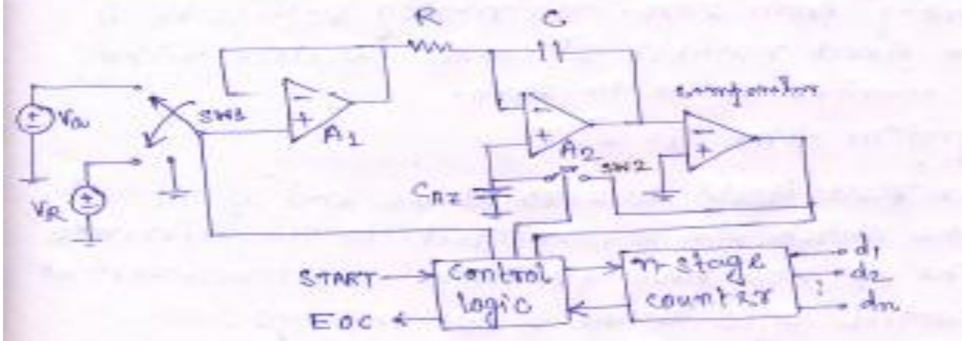


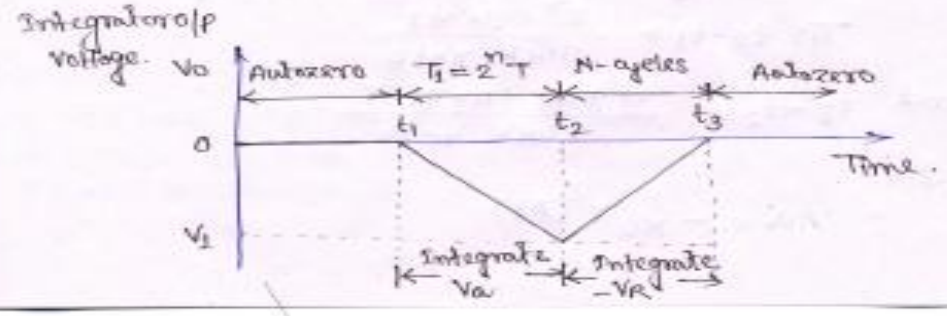
Functional diagram of the successive approximation ADC

The conversion sequence for a typical analog input is shown below.

correct digital representation	successive approximation resistor output Vd at different stages in conversion	comparator output
11010100	10000000	1
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Dual slope ADC





4

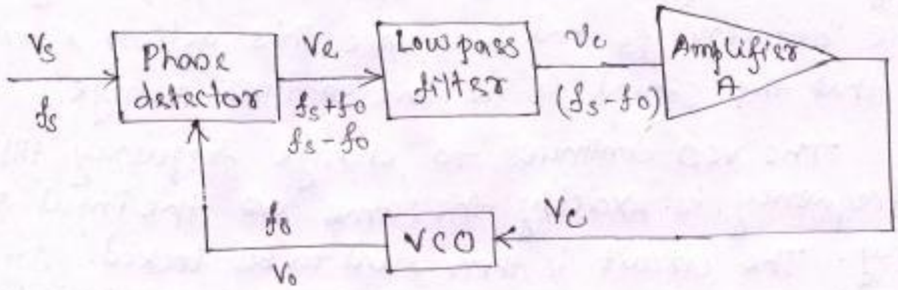
Phase-locked loop (PLL)

Phase-locked loop is an important building block of linear systems. PLLs are available as inexpensive monolithic IC. NE565 is the IC for PLL.

Basic principles

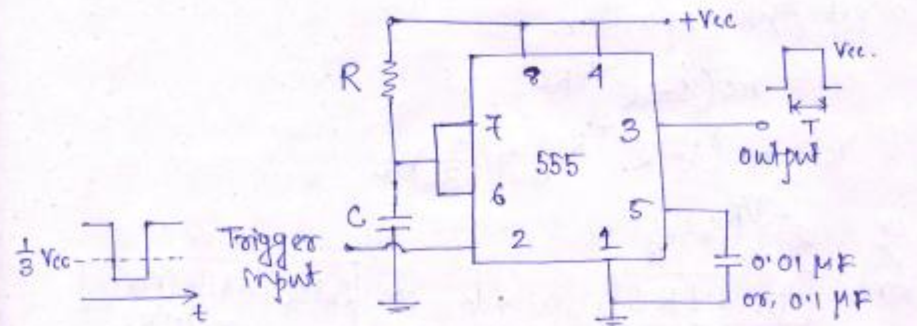
The basic block schematic of the PLL is shown. The feedback system consists of

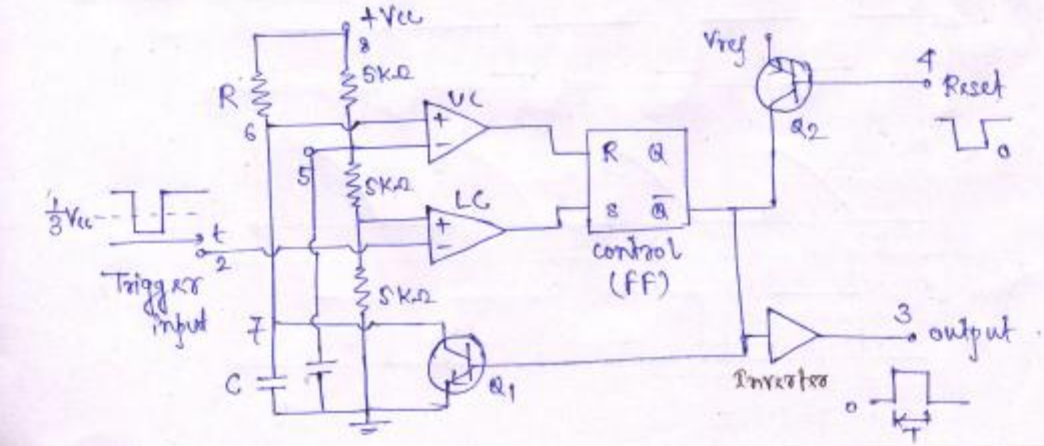
(i) Phase detector/comparator.
(ii) A low pass filter.
(iii) An error amplifier
(iv) A voltage controlled oscillator.



5.

Monostable Multivibrator





6.

Solution

$$f = \frac{1.45}{(R_A+2R_B)\,C} = 1\times10^3$$

or, $(R_A+2R_B)\times 0.1\times10^{-6} = \frac{1.45}{1\times10^3}$ [~~Assume~~ Select, $C = 0.1\,\mu F$]

or, $R_A+2R_B = 14.5\times10^3 = 14.5\ K\Omega$. ——(1)

$$D = \frac{R_A+R_B}{R_A+2R_B} = 0.6$$

or, $R_A+R_B = 0.6\,(R_A+2R_B) = 0.6\times14.5\ K\Omega$

$= 8.7\ K\Omega$. ——(2)

~~Let~~ Using eq (1) and (2) we get,

$R_B = (14.5 - 8.7)\ K\Omega = 5.8\ K\Omega \simeq 5.6\ K\Omega$

$R_A = 8.7 - 5.6 = 3.1\ K\Omega \simeq 3.3\ K\Omega$.