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08EC082

M.Tech. Degree Examination, December 2011
VLSI Systems and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. What is an instruction set architecture [ISA]? List and brief the different types of ISA's based on operand addressing field. Illustrate the code sequence for C = A + B for each ISA type. **(10 Marks)**

b. What is virtual memory? Illustrate its organization and demand paging. **(10 Marks)**

2 a. Explain the different DLX instruction formats. Also mention the DLX control flow instructions, with an example each. **(10 Marks)**

b. Give the differences between micro programmed and hard wired control units, with the functional block diagrams for each. **(10 Marks)**

3 a. List different hazards present in the pipeline. Make a difference between any two of them. **(10 Marks)**

b. What are register and cache windows? Mention the major differences between them. **(10 Marks)**

4 a. How would this loop be scheduled on a superscalar pipeline for MIPS?

```
Loop : lw $ to, 0 ($ S1) # $ to = array element
       addu $ to, $ to, $ S2 # add scalar in $ S2
       SW $ to, 0 ($ S1) # stone result
       addi $ S1, $ S1, -4 # decrement pointer
       bne $ S1, $ zero loop # branch $ S1 1 = 0.
```

Reorder the instructions to avoid as many pipeline stalls as possible. **(08 Marks)**

b. Assume a cache of 4k blocks and a 32 bit address. Find the total number of sets and the total number of tag bits for caches that are direct mapped, two way and 4 – way set associative and fully associative. **(12 Marks)**

5 a. Differentiate between super scalar architecture and VLIW architecture. Brief the limitation on parallel execution. **(10 Marks)**

b. Compare the typical features of RISC and CISC architecture. Explain the addressing mode, operand sizes and instruction encoding for any one of the RISC processors. **(10 Marks)**

6 a. List the bit field instructions of Motorola 68000, with their functions. **(10 Marks)**

b. Explain the addressing modes of any DSP processor, with neat illustrations. **(10 Marks)**

7 a. Illustrate synthesis problem, with an example. **(10 Marks)**

b. How an resource is shared in pipeline? Explain for a scheduling with pipelined resources. **(10 Marks)**

8 a. Consider 7 intermediate variables {2i, 22i = 1, 2, ...7}, 3 loop variables (x, y, u) and 3 loop variants (a, 3, dx). Construct the sequencing graph, variable life time and lift time as axes on a circle by considering register sharing. **(12 Marks)**

b. Explain testable resources and their types briefly. **(08 Marks)**

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