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08EC082

M.Tech. Degree Examination, June/July 2011
VLSI System and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain the lower bounds on VLSI circuits for implementing parallel algorithms with VLSI chips. **(10 Marks)**

b. What is cache memory? Explain with illustration direct and 4-way set associative mapping techniques. **(10 Marks)**

2 a. What do you mean by instruction encoding? What factors are considered while encoding instruction set? Explain the different encoding scheme by giving their general format. **(10 Marks)**

b. With a neat diagram, explain a 2-bit branch prediction scheme. **(10 Marks)**

3 a. Give the format for microinstruction and explain the fields. **(10 Marks)**

b. Design a 2's compliment multiplier using state table method. **(10 Marks)**

4 a. Explain the 5 implementation stages for the DLX architecture with relevant block diagram. **(10 Marks)**

b. Given an unpipelined processor with a 10 ns cycle time and pipeline latches with 0.5 ns latency. What are the cycle times of pipelined version of the processor with 2, 4, 8 stages if the data path logic is evenly divided among the pipeline stages? For the same processor how many stages of pipelining are required to achieve a cycle time of 2 ns and 1 ns? **(10 Marks)**

5 a. Explain dynamic scheduling with Tamasuco's algorithm. **(10 Marks)**

b. Explain instruction-level parallelism with various types of dependencies giving illustration for each. **(10 Marks)**

6 a. What is pipelining? Discuss how pipelining is used in superscalar, super pipelined and VLIW architectures. **(10 Marks)**

b. For a processor with base CPI of 1.0, assuming all references hit in the primary cache, and a clock rate is 5 GHz. Assume a main memory access time of 100 ns, including all the miss handling. If the miss rate per instruction at the primary cache is 2%, how much faster will the processor be if we add a secondary cache with 5 ns access time and is large enough to reduce the miss rate to main memory to 0.5%? **(10 Marks)**

7 a. With the help of a block diagram, explain the features of the TMSC5X DSP processor. **(10 Marks)**

b. Discuss resource allocation with respect to a DSP processor. What are various mechanisms in which resource allocation is done? **(10 Marks)**

8 a. List and explain the memory addressing modes of a TMS 320 C5X DSP processor. **(10 Marks)**

b. Discuss the purpose of scheduling operation for DSP. Explain various scheduling techniques. **(10 Marks)**

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