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10EC130

M.Tech. Degree Examination, December 2011
VLSI Design Verification

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. With respect to SOC design flow, explain the need of verification. **(06 Marks)**

b. For the following code, generate the code coverage analysis: **(14 Marks)**

```
L1:  always@(current_State or areq1 or areq0 or rid)
L2:  begin
L3:     next_state = idle;
L4:     case(current_state)
L5:        idle:
L6:           if ((areq1= = 1 && areq0 = = 0) or (areq0 = = 1 &&
                  areq1 = = 1 && rid = = 2'b01))
L7:              next_state = master2;
L8:           else if((areq0 = = 1 && areq1 = = 0) or (areq0 = = 1 &&
                        areq1 = = 1 && rid = = 2'b00))
L9:              next_state = master1;
L10:          else
L11:             next_state = idle;
L12:       master1:
L13:          if (areq1= = 1)
L14:             next_state = master2;
L15:          else if (areq1 = = 0 && areq0 = = 0)
L16:             next_state = idle;
L17:          else
L18:             next_state = master1;
L19:       master2:
L20:          if (areq0 = = 1)
L21:             next_state = master1;
L22:          else if (areq1 = = 0 && areq0 = = 0)
L23:             next_state = idle;
L24:          else
L25:             next_state = master2;
L26:    endcase
L27: end
```

2 a. Distinguish between testing, verification and post-silicon validation. **(08 Marks)**

b. What is the need of test benches in the system level verification? Write a test bench to test for functional verification of a 3-bit Mod 6 counter. **(12 Marks)**

3 a. Explain the mixed signal simulation environment with respect to selection and limitations. Also explain the parameters involved into perform simulation, using SPICE. **(10 Marks)**

b. For the below property specifications of an arbiter ASB|APB bridge of Bluetooth SOC, execute model checking for the mentioned property details, with respect to constraints and state variables.

i) Liveness property of arbiter
After(arbiter · areq0 = = 1) eventually(arbiter · agnt0 = = 1)

ii) Mutual exclusive property of arbiter
Never((arbiter · agnt0 + arbiter · agnt1 + arbiter · agnt2) > 1)

iii) Pstb single property of ASB|APB brige
After(bridge·pstb = = 1 && bridge·bclk = = rising)
Never(Clock_tick_count > 1)

iv) Pselx signal line property with reference to Pstb line of ASB|APB bridge
After(bridge·pstb = = rising)
Never(bridge·pselx[X] = = rising || bridge·pselx[X] = = falling)
Unless After(bridge·pstb = = falling) **(10 Marks)**

4 a. Distinguish between EBS and CBS. **(10 Marks)**

b. Explain the emulation with respect to environment, selection and limitations. **(10 Marks)**

5 a. Write a detailed note on the rapid prototyping systems. **(10 Marks)**

b. Mention the guidelines and methodology of FPGA based design. **(10 Marks)**

6 a. With respect to perform, selection, methodology and guidelines, explain the static timing verification. **(10 Marks)**

b. In DSM design, on which issues physical effects will be analyzed? Explain briefly. **(10 Marks)**

7 a. With a neat diagram, explain the model checking approach. **(10 Marks)**

b. Explain the first order logic of formal systems. **(10 Marks)**

8 Write short notes on:

a. Binary decision diagrams

b. IP reuse. **(10 Marks)**

c. Equivalence checking **(10 Marks)**

d. White, black and gray box testing.

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