CS/IS6D2

USN | | | | | | | | | | |

Sixth Semester B.E. Degree Examination, July/August 2003

Computer Science / Information Science & Engg.

VLSI Design

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) Explain the four important advantages of VLSI. (8 Marks)
   (b) State Moore Law and discuss. (4 Marks)
   (c) Describe the hierarchy of design abstraction for IC's. (8 Marks)

2. (a) Explain latch up in MOS transistor and explain how it is avoided. (8 Marks)
   (b) Define the terms :
   i) Wafer ii) Mask iii) Polysilicon iv) Diffusion. (4 Marks)
   (c) Sketch a layout diagram for two input CMOS NAND gate and indicate metal, polysilicon and diffusion region. (4 Marks)
   (b) Design the static complimentary pull up and pull down networks for the following logic expression.
   i) $y = (\overline{a+b+c})$ ii) $y = (\overline{a+b})c$ (4 Marks)

3. (a) Bring out a model to analyze a delay of simple inverter with necessary assumption. (8 Marks)
   (b) Derive an equation to determine the dynamic power consumption for a CMOS inverter. What is speed power product? (12 Marks)

4. (a) Using the concept of single row layout design, explain the layout design of a full adder. (10 Marks)
   (b) Explain varying degrees of cross talk coupling between signals. Discuss the methods to minimize cross talk. (10 Marks)

5. (a) Discuss the testing of logic gates using fault model concept. (8 Marks)
   (b) Explain the clocking discipline of a sequential system. Discuss the two phase clocking strategy used to operate latches. (12 Marks)

6. (a) Explain the concept of pipe lining in combinational logic network. (10 Marks)
   (b) What is a barrel shifter? Explain its operation with a neat schematic. (10 Marks)

7. (a) Design three transistors and one transistor DRAM core cells and explain their operation. Compare the performance with one another. (10 Marks)
   (b) Briefly describe floor planning, block placement and channel definition. (10 Marks)

8. Write short notes on :
   i) Data path controller architecture. (7 Marks)
   ii) A generic design flow for VLSI systems. (7 Marks)
   iii) Technology dependent logic optimization. (6 Marks)

** * **

CS/IS6D2

USN | | | | | | | | | | |

Sixth Semester B.E. Degree Examination, January/February 2004

Computer Science / Information Science & Engg.

VLSI Design

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) What are the advantages of integrated circuits over discrete components? Why FETs are preferred over BJTs in VLSI? **(8 Marks)**

   (b) With examples explain design abstraction for integrated circuits. **(7 Marks)**

   (c) What are layout design rules? Give any three examples. **(5 Marks)**

2. (a) Explain VLSI fabrication steps with neat schematics. **(10 Marks)**

   (b) Describe V-I characteristics of NMOS transistor. Give the simple transistor current equations and explain the parameters involved. **(10 Marks)**

3. (a) Write a note on 'yield statistics'. **(5 Marks)**

   (b) Calculate resistance and capacitance of following polysilicon wire shown in Fig 3(b).

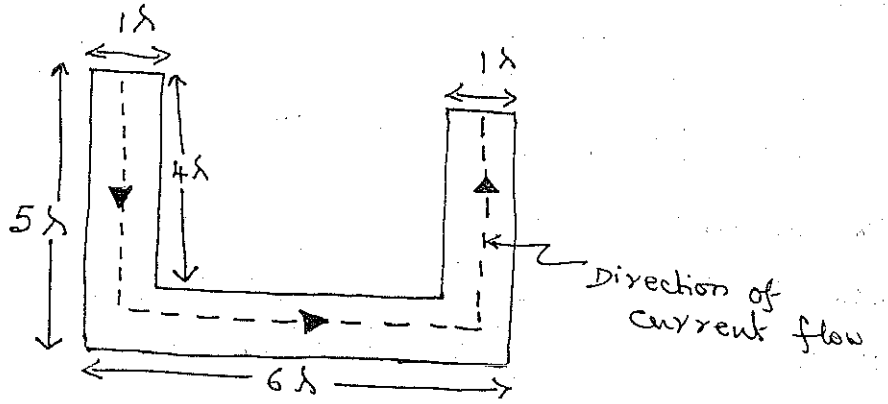

Fig. 3(b)

Given : Resistivity = $4\Omega/\square$
Plate capacitance = $0.09fF/\mu m^2$
Fringe capacitance = $0.04fF/\mu m$
Process used = 2 micron process $(= 2\lambda)$

(15 Marks)

Contd.... 2

4. (a) Give the circuit diagram and stick diagram for 3 input CMOS OR gate. **(6 Marks)**

(b) How is the delay estimated in CMOS inverter? Explain with necessary equations. **(6 Marks)**

(c) What is the minimum inverter delay assuming : Wire capacitance connecting o/p of the inverter to the load is 500Ω; $C_g = 0.9fF/\mu m^2$; Capacitive load = one minimum size transistor's gate capacitance; process used = 0.5 micron process. **(8 Marks)**

5. (a) Explain left edge channel routing algorithm with an example. **(8 Marks)**

(b) What is a CMOS switch? Draw the circuit of a 2:1 multiplexer using CMOS switch logic. **(8 Marks)**

(c) Define :

i) Controllability

ii) Observability in VLSI circuits. **(4 Marks)**

6. (a) Draw the logic diagram and CMOS circuit diagram of a SR flipflop. **(8 Marks)**

(b) Write notes on

i) Design for testability ii) Automatic test pattern generator. **(6 Marks)**

(c) What is a field programmable gate Array? What are its advantages and limitations? **(6 Marks)**

7. (a) What is meant by floor planning? Discuss various issues involved in floor planning. **(8 Marks)**

(b) What is meant by synthesis? Discuss various jobs of high level synthesis. **(6 Marks)**

(c) What is an ASM chart? Explain. **(6 Marks)**

8. (a) What is a simulator? What are different types of simulators? Explain. **(8 Marks)**

(b) Describe the Greedy channel router. **(6 Marks)**

(c) Describe various operations performed by a logic synthesizer. **(6 Marks)**

** * **