2002 SCHEME

USN | | | | | | | | | | |

EC74

Seventh Semester B.E. Degree Examination, June/July 2011
VLSI Circuits

Time: 3 hrs. Max. Marks:100

Note: 1. ***Answer any FIVE full questions.***
2. ***Missing data may be suitably assumed.***

1 a. Explain the importance of full custom and semicustom design styles upon the design cycle time and achievable circuit performance. **(06 Marks)**

b. Write the node voltages equations at nodes V_1, V_2 and V_3 for fig. Q1(b)(i) and fig. Q1(b)(ii).

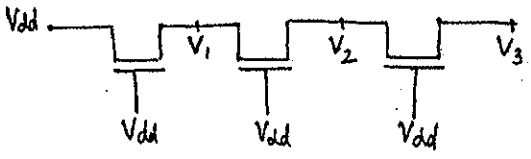

Fig. Q1(b)(i)

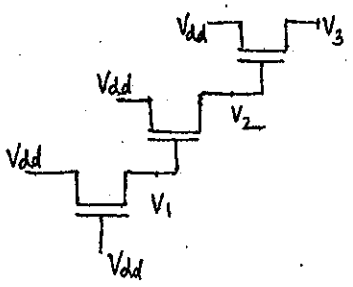

Fig. Q1(b)(ii)

Assume the threshold voltage of each of the transistor to be V_{tn}. **(06 Marks)**

c. Design 4 : 1 Mux using transmission gates. Also write the advantages and disadvantages of transmission gates. **(08 Marks)**

2 a. Design a CMOS logic gate for the function: $f = \overline{(a \cdot b + a \cdot c + b \cdot d)}$ using the smallest number of transistors. **(04 Marks)**

b. Derive the expression for the linear resistance R_n of nFET. **(06 Marks)**

c. Draw the stick diagram layout for the Boolean function $z = \overline{(A(D+E)+BC)}$ using Euler path approach. **(10 Marks)**

3 a. Discuss drawn and effective dimensions of MOSFET. **(04 Marks)**

b. Write a note on design hierarchies. **(08 Marks)**

c. Design the circuit and layout for a CMOS gate that implements the function, $F = \overline{(a \cdot b \cdot c + a \cdot d)}$ using the fewest number of transistors and a compact layout style. **(08 Marks)**

4 a. Explain the five regions of VTC of an inverter. Also, derive the midpoint voltage equation V_m for the same. **(12 Marks)**

b. Find the total capacitance at the output for the fig. Q4 (b). The give parameter are, $L = 1\ \mu m$ (drawn), $L_0 = 0.1\ \mu m$, $V_{dd} = 5\ V$, $C_{ox} = 2.70\ fF/\mu m^2$

$pFET: k_p' = 60\,\mu A/V^2$ $\quad nFET: k_n' = 150\,\mu A/V^2$

$V_{TOp} = -0.7\ V$ $\quad V_{TOn} = 0.6\ V$

$G = 1.05\ fF/\mu m^2$ $\quad G = 0.86\ fF/\mu m^2$

$G_{sw} = 0.32\ fF/\mu m$ $\quad G_{sw} = 0.24\ fF/\mu m$ **(08 Marks)**

Q4 (b) Contd....

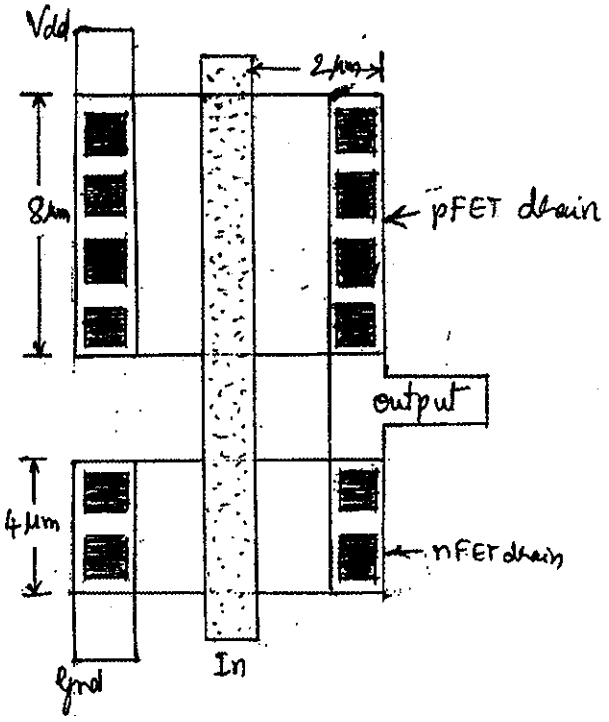

Fig. Q4 (b)

5 a. Explain different types of power dissipation taking place in a CMOS inverter. **(06 Marks)**

b. A CMOS NAND2 is designed using identical nFETs with a value of $\beta_n = 2\beta_p$; the pFETs are the same size. The power supply is chosen to be Vdd = 5 V and the device threshold voltages are given as $V_{tn} = 0.60$ V and $V_{tp} = -0.70$ V.

i) Find the midpoint voltage V_m for the case of simultaneous switching.

ii) What would be the midpoint voltage for an inverter made with the same β - specification? **(06 Marks)**

c. Derive the rise time and fall time equations for NAND2 gate. **(08 Marks)**

6 a. Derive the minimized total delay equation in an inverter cascade to drive large capacitive load. **(12 Marks)**

b. Design a digital BicMOS circuit that implements the function of NAND2 gate. Also discuss the dependence of cMOS and BicMOS circuits on gate delay and external load capacitance. **(05 Marks)**

c. Define : i) Logical effort ii) Electrical effort iii) Absolute delay time **(03 Marks)**

7 a. Explain the cascading problem in dynamic cMOS logic circuit. **(05 Marks)**

b. Draw the pseudo-nMOS circuit that provide the logic operation, $f = \overline{(a \cdot b + c)}$. **(04 Marks)**

c. Explain mirror circuits with example. **(08 Marks)**

d. Explain the term charge sharing. **(03 Marks)**

8 Write short notes on:

a. General overview of design hierarchy. **(07 Marks)**

b. Clocking and data flow control. **(07 Marks)**

c. Clocked cMOS. **(06 Marks)**

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