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06EE766

Seventh Semester B.E. Degree Examination, December 2011
VLSI Circuits and Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. With a neat diagram, explain the structure of an NMOS enhancement mode transistor. **(05 Marks)**

b. With the help of necessary structures, explain the p-well CMOS fabrication process. **(10 Marks)**

c. With a graphical representation, discuss the relative gate delay and relative cost per gate of BiCMOS, ECL, CMOS and GaAs technologies. **(05 Marks)**

2 a. Using neat diagrams, explain the latch up phenomenon in a p-well CMOS inverter. **(10 Marks)**

b. Explain the operation of a CMOS inverter in different regions of its transfer characteristic. Also, draw the graph of inverter current versus input voltage. **(05 Marks)**

c. With a neat circuit diagram, explain the working of improved version of BiCMOS inverter configuration for a better output logic levels. **(05 Marks)**

3 a. Draw the transistor level circuit and stick diagram of an inverting type NMOS shift register cell. Clearly indicate the monochrome codes used for the stick diagram. Also, draw its optimum layout diagram indicating the dimensions of the MOS layers. **(10 Marks)**

b. Using neat diagrams, express the lambda based design rules as applicable to MOS layers, transistors and contact cuts. **(10 Marks)**

4 a. An off chip capacitive load of 20 PF is to be driven by a chain of CMOS inverters of 5μm technology. Compute the number of inverters width factor and coverall delay through the chain of inverters for minimum overall delay. Assume square capacitance for 5 μm technology as 0.01 PF and sheet resistance as 10 kohms. **(10 Marks)**

b. With a neat diagram, explain the working of an inverting type NMOS superbuffer. **(05 Marks)**

c. Write a short note on BiCMOS drivers. **(05 Marks)**

PART – B

5 a. With a neat diagram, explain the concept of scaling in a MOS transistor. **(05 Marks)**

b. Determine the scaling factors for the following MOS transistor parameters. Use constant electric field scaling model.
i) Gate capacitance ii) Channel resistance iii) Gate delay
iv) Saturation current v) Current density. **(10 Marks)**

c. How the propagation delay can be estimated for a typical metal interconnection model? Explain. **(05 Marks)**

6 a. With a suitable example, explain the concept of dynamic CMOS logic. **(08 Marks)**

b. Explain the structured design approach for a parity generator circuit. Draw the NMOS stick diagram of its basic cell. **(07 Marks)**

c. Draw and explain a combinational circuit to generate two phase clocking. **(05 Marks)**

7 a. List the general considerations for the VLSI design. **(03 Marks)**

b. With neat diagrams, explain the basic bus architecture for a 4-bit arithmetic processor. **(10 Marks)**

c. Draw a neat diagram of a 4×4 barrel shifter. Explain its operation. **(07 Marks)**

8 a. Define regularity. Explain its significance by considering an example. **(04 Marks)**

b. Draw the structure of a multiplexer based adder logic with stored and buffered sum output. **(04 Marks)**

c. With a neat diagram and relevant expressions, explain the implementation of ALU functions, using the adder elements. **(12 Marks)**

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