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06EE766

Seventh Semester B.E. Degree Examination, May/June 2010
VLSI Circuits and Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Bring out the salient features of fabrication of P-well CMOS inverter. **(08 Marks)**

b. What are the differences between CMOS and bipolar technology? **(04 Marks)**

c. Derive an expression for Ids in non-saturated region of MOS device. **(08 Marks)**

2 a. Show that pull up-to-pull down ratio for nMOS inverter driven through one or more pass transistor, is $\frac{Z_{pu2}}{Z_{pd2}} = 8:1$. **(08 Marks)**

b. Explain the working of Bi-CMOS inverter with and without static current flow. **(06 Marks)**

c. With a circuit, explain two different forms of pull up for inverter. **(06 Marks)**

3 a. Discuss the latch up in CMOS with p-well or n-well structure. **(06 Marks)**

b. Bring out λ based nMOS design rules, with examples. **(06 Marks)**

c. Bring out micron rules for CMOS with examples, giving the difference between buried and butting contact. **(08 Marks)**

4 a. What is sheet resistance? Calculate sheet resistance of transistor channel if $L = 8\lambda$, $W = 2\lambda$ if n transistor channel $R_S = 10^4$ Ω/square. **(04 Marks)**

b. Derive an expression for rise time and fall time of CMOS inverter. **(06 Marks)**

c. For cascaded inverters as drivers for large capacitive loads, show that minimum delay for given $y = C_L / \square C_g = f^N$, if $f = e$, where f is the width of the inverter, N is number of stages. What are super buffer buffers? Explain. **(10 Marks)**

PART – B

5 a. Calculate the area capacitance for the following structure if relative capacitances are,
i) Metal 1 to substrate 0.075×10^{-4} pF/μm^2. ii) Polysilicon to substrate 0.1×10^{-4} pF/μm^2
iii) Gate to channel $1\,pF \times 10^{-4}$ pF/μm^2. **(07 Marks)**

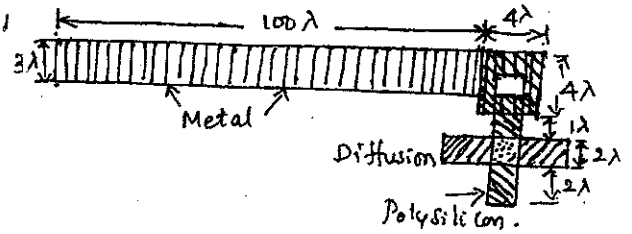

Fig. Q5 (a)

b. For combined voltage and electric field scaling, find scaling factors in terms of α, β for the following parameters : i) Gate capacitance ii) Maximum operating frequency f_o
iii) Saturation current I_{dss} iv) Switching energy per gate E_g. **(08 Marks)**

c. Discuss limitations of scaling for interconnect and contact resistance. **(05 Marks)**

6 a. For a combined voltage and electric field scaling, show that the scaling factor for effective voltage Va is $(m+\beta)/\beta(m+1)$ where m is a real number. **(06 Marks)**

b. What are the guidelines for a subsystem design process? Bring out the merits and demerits between pass transistor and transmission gate. **(08 Marks)**

c. What are the limitations of sub-threshold current scaling and current density? **(06 Marks)**

7 a. Why NOR gate structure is preferred to NAND for nMOS? Derive an expression for Z_{pu}/Z_{pd} ratio for NAND and NOR gate. **(06 Marks)**

b. Explain the pseudo nMOS and CMOS domino logic showing the difference between the two. **(08 Marks)**

c. Give the structured design of bus arbitration logic for n-line bus. **(06 Marks)**

8 a. Discuss the current limitations for VDD and GND rails. **(04 Marks)**

b. For 4 bit arithmetic processor, explain any two architectures. **(06 Marks)**

c. Give the regular design of an adder cell and show how arithmetic and logical functions are implemented using adder cell. **(10 Marks)**

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