

Seventh Semester B.E. Degree Examination, Dec.2014/Jan.2015

VLSI Circuits & Design

Time: 3 hrs.

Max. Marks:100

**Note: 1. Answer FIVE full questions, selecting at least TWO questions from each part.
2. Missing data suitably assumed.**

PART - A

- 1 a. Discuss Moore's law, with graph. (04 Marks)
b. Compare speed / power performance of available IC technologies. (06 Marks)
c. Explain in detail the process of Nmos fabrication with neat diagrams. (10 Marks)
- 2 a. Discuss drain-to-source current versus voltage relationships for non-saturated and saturated regions. (10 Marks)
b. Define Z_{pu} and Z_{pd} . Show that pull-up to pull-down ratio for Nmos inverter driven through one or more pass transistors is, $\frac{Z_{pu2}}{Z_{pd2}} = 8 : 1$ (10 Marks)
- 3 a. Write a note on MOS layers. (04 Marks)
b. Draw circuit symbols and stick diagrams of, i) NMOS ii) CMOS inverter. (10 Marks)
c. Draw the stick diagram and layout for an NMOS two way selector, with enable input. (06 Marks)
- 4 a. What is area capacitance and standard unit of capacitance? Calculate the total area capacitance for the multilayered structure shown in Fig. Q4 (a). Assume for $5\mu\text{m}$ technology:
i) Metal 1 to substrate : $0.075 \times 10^{-4} \text{ pF}/\mu\text{m}^2$.
ii) Polysilicon to substrate : $0.1 \times 10^{-4} \text{ pF}/\mu\text{m}^2$.
iii) Gate to channel : $1 \times 10^{-4} \text{ pF}/\mu\text{m}^2$. (10 Marks)

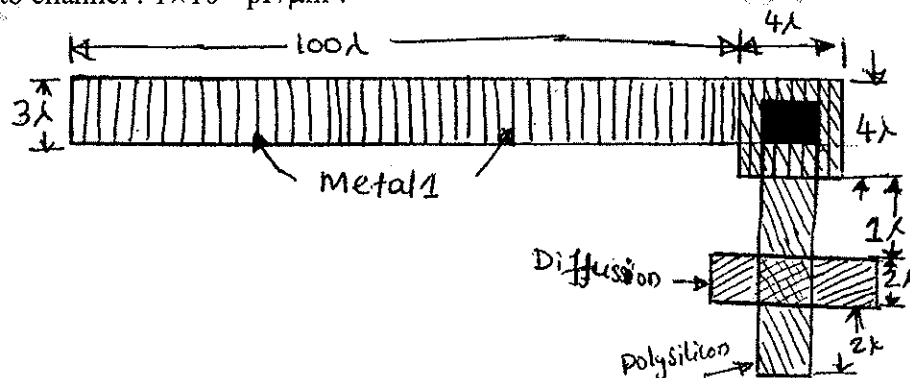


Fig. Q4 (a)

- b. Derive an expression for rise time and fall time of CMOS inverter. (06 Marks)
- c. What is sheet resistance? Calculate sheet resistance of transistor channel if $L = 8\lambda$, $W = 2\lambda$, if n-transistor channel $R_s = 10^4 \Omega/\text{square}$. (04 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – B

- 5 a. What are the different scaling models and scaling factors? Draw scaled nMOS transistor diagram. (08 Marks)
- b. Indicate scaling factors for,
 i) Gate area ii) Gate capacitance iii) Gate delay iv) Current density
 v) Power speed product vi) Channel resistance. (06 Marks)
- c. Write a note on limitations of scaling. (06 Marks)
- 6 a. Explain in detail: i) Pseudo-nMOS logic and ii) Dynamic CMOS logic. (10 Marks)
- b. Explain the structured design of bus arbitration logic for n lines. Also, write the circuit diagram and the stick diagram for a single cell. (10 Marks)
- 7 a. Explain the general arrangement of a 4-bit arithmetic processor. (10 Marks)
- b. Explain the operation of 4×4 cross bar switch with a neat diagram. (10 Marks)
- 8 a. Explain the some observations on the design process. (06 Marks)
- b. What is regularity? Explain. (04 Marks)
- c. With a neat diagram and relevant expressions, explain the implementation of a 4 bit Alu, using full adders. (10 Marks)
