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10EE764

Seventh Semester B.E. Degree Examination, Dec.2013/Jan.2014
VLSI Circuits & Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the nMOS fabrication process with neat diagram. **(10 Marks)**

b. Discuss Moore's law, with graph. **(02 Marks)**

c. Compare the characteristics of cMOS and bipolar technologies. **(08 Marks)**

2 a. Define $Z_{p.u}$ and $Z_{p.d}$. Show that pull up to pull down ratio for nMOS inverter driven through one or more pass transistor, is $\frac{Z_{pu2}}{Z_{pd2}} = 8:1$. **(10 Marks)**

b. Explain the latch-up phenomena in cMOS circuits. **(05 Marks)**

c. With neat diagrams, explain the merits and demerits of BiCMOS inverter configurations. **(05 Marks)**

3 a. Draw the stick diagram and layout for an nMOS two way selector, with enable input. **(06 Marks)**

b. Define stick diagram. Explain the encodings used for a simple nMOS process. **(06 Marks)**

c. With relevant diagrams, explain the Lambda based design rules as applicable to p-well cMOS process. **(08 Marks)**

4 a. What is silicide? Discuss the advantages and disadvantages of using it inplace of polysilicon. **(06 Marks)**

b. What is sheet resistance? Calculate sheet resistance of transistor channel if L = 8λ, W = 2λ, if n transistor channel $R_S = 10^4\ \Omega$ / square. **(06 Marks)**

c. Calculate the area capacitance for the following structure if relative capacitances are :

i) Metal 1 to substrate 0.0754×10^{-4} pF/μm^2.

ii) Polysilicon to substrate 0.1×10^{-4} pF/μm^2

iii) Gate to channel 1×10^{-4} pF/μm^2. **(08 Marks)**

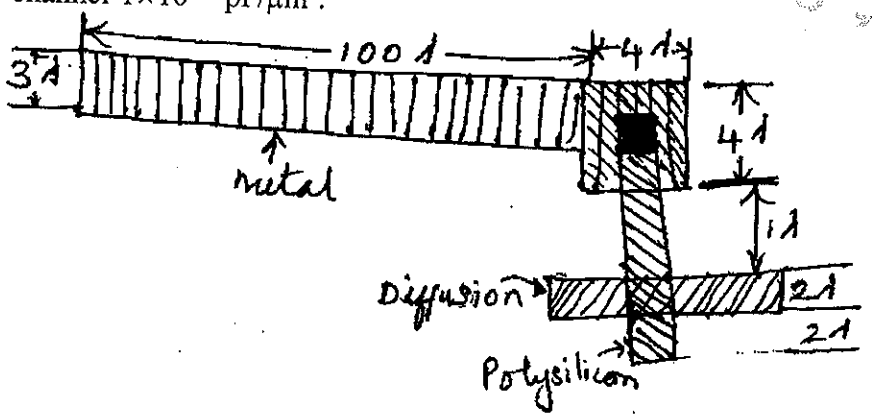

Fig. Q4 (c)

PART – B

5 a. List the scaling factors for device parameters. **(14 Marks)**

b. Discuss limitations of scaling for interconnect and contact resistance. **(06 Marks)**

6 a. What are the guidelines for a subsystem design process? Bring out the merits and demerits between pass transistor and transmission gate. **(08 Marks)**

b. Write the structure and stick diagram of cMOS, BicMOS two input NOR gate. **(08 Marks)**

c. Explain in detail pseudo-nMOS logic. **(04 Marks)**

7 a. Explain the operation of 4×4 cross bar switch with a neat diagram. **(10 Marks)**

b. Explain the design of an ALU subsystem. **(10 Marks)**

8 Write short notes on:

a. Super buffers.

b. Basic bus architectures.

c. Two phase clock generator using 'D' flip-flops.

d. Dynamic register element. **(20 Marks)**

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