USN | | | | | | | | | | |

06EE766

Seventh Semester B.E. Degree Examination, June/July 2011
VLSI Circuits and Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. With neat diagrams, explain the process of P-well CMOS fabrication in detail. **(07 Marks)**

b. Explain briefly, with neat diagrams, the arrangement of Bi CMOS bipolar transistor. **(06 Marks)**

c. Explain the procedure used for the production of E-beam mask. What are the advantages of using the E-beam mask? **(07 Marks)**

2 a. What is meant by $Z_{p.u}$ and $Z_{p.d}$? Derive the required ratio between $Z_{p.u}$ and $Z_{p.d}$ if an nMOS inverter is driven through one or more pass transistors. **(07 Marks)**

b. Explain the operation of nMOS inverter in detail. Derive the nMOS inverter transfer characteristics from the output characteristics of enhancement and depletion mode transistors. **(07 Marks)**

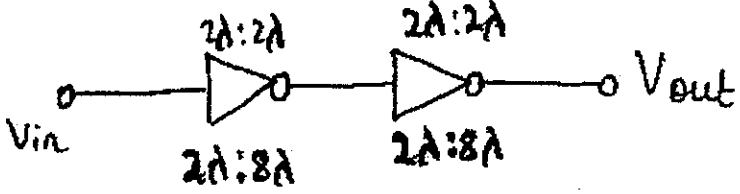
c. Explain the operation of a Bi CMOS inverter with a neat circuit diagram. Also explain how a Bi CMOS inverter can be improved to provide better output logic levels. **(06 Marks)**

3 a. What are stick diagrams? Explain the encodings used for a simple nMOS process. **(06 Marks)**

b. With relevant diagrams, explain the Lambda (λ) based design rules as applicable to wires, transistors and contacts. **(10 Marks)**

c. Draw the stick diagram for 4:1 nMOS inverter and 1:1 CMOS inverter. **(04 Marks)**

4 a. Consider the nMOS inverter circuit shown in Fig. Q4 (a). If twenty five (25) such pairs are connected in cascade, find the total delay for 5μm technology.



(06 Marks)

b. Estimate the CMOS inverter delay in terms of rise time and fall time. **(08 Marks)**

c. Show that the delay is minimum when f = e (base of natural logarithms) where f is the width factor when N number of nMOS inverters connected in cascade are driving large capacitive load C_L. **(06 Marks)**

PART – B

5 a. Derive the scaling factors for the following device parameters by considering constant electric field scaling model i) Gate capacitance ii) Channel resistance iii) Saturation current iv) Frequency of operation. **(08 Marks)**

b. Explain in detail the limitations of scaling. Also, discuss the advantages of scaling. **(12 Marks)**

6 a. Explain in detail i) pseudo-nMOS logic and ii) Dynamic CMOS logic. **(10 Marks)**

b. Explain the structured design of bus arbitration logic for n lines. Also, write the circuit diagram and the stick diagram for a single cell. **(10 Marks)**

7 a. Explain how a four –way multiplexer can be used to develop a General logic function block of two variables. **(06 Marks)**

b. Draw the circuit diagram and the stick diagram for two input nMOS NOR gate and explain its operation. **(06 Marks)**

c. Explain with neat diagrams, the working of inverting and non-inverting dynamic storage cells. **(08 Marks)**

8 a. Explain the operation of 4 × 4 cross-bar switch with a neat circuit diagram. **(10 Marks)**

b. Design a multiplexer based adder logic with stored and buffered sum output. Draw the stick diagram. **(10 Marks)**

* * * * *