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06EE766

Seventh Semester B.E. Degree Examination, December 2010
VLSI Circuits and Design

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions, selecting at least TWO questions from each part.*
2. Any missing data may be assumed suitably.

PART – A

1 a. With neat diagrams, explain the working of enhancement mode NMOS transistor, for different values of V_{DS}. **(08 Marks)**

b. What are the advantages if N-well CMOS circuits? List the main steps involved in N-well CMOS fabrication. **(06 Marks)**

c. Draw the structure of a P-well CMOS inverter. Neatly label the parts. **(06 Marks)**

2 a. Show that pull-up to pull-down ratio for an NMOS inverter, driven through one or more pass transistors, is 8:1. **(10 Marks)**

b. With neat circuit diagrams, explain the merits and demerits of BiCMOS inverter configurations. **(10 Marks)**

3 a. Draw the stick diagram and layout for an NMOS two way selector, with enable input. **(06 Marks)**

b. What are design rules? Give the significance of lambda based design rules. With neat diagrams, explain lambda based design rules as applicable to MOS layers and transistors. **(08 Marks)**

c. What are the advantages of a complementary transistor pull-up, for an inverter? With relevant diagrams, explain the CMOS inverter operation in different regions. **(06 Marks)**

4 a. Calculate the resistance between V_{DD} and V_{SS} of an NMOS inverter with pull – up to pull – down ratio = 4 and show that the ratio rule does not apply for CMOS inverter. Take lambda = 5 μm. **(06 Marks)**

b. Calculate the total capacitance in pico farads between the substrate and the structure shown in Fig.Q.4(b) for lambda = 5 μm. Use standard values. **(08 Marks)**

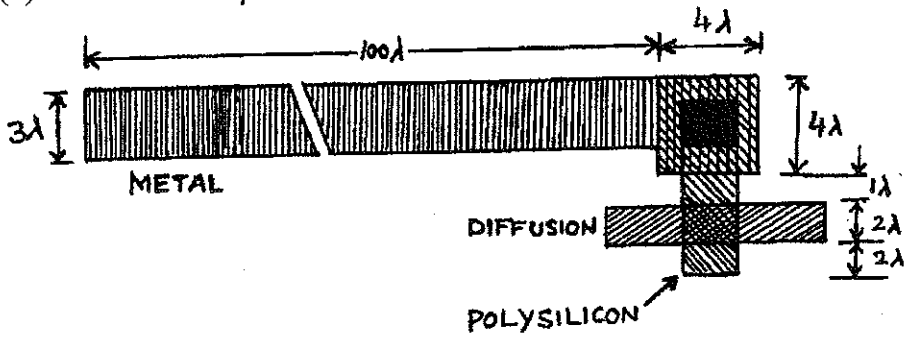

Fig.Q.4(b).

c. Give the concept of sheet resistance, square capacitance and delay unit. **(06 Marks)**

PART – B

5 a. Explain different scaling models by considering the relevant diagram of an NMOS transistor. **(06 Marks)**

b. Obtain the scaling factors for the following transistor parameters, by considering the constant voltage scaling model :
   i) Gate area
   ii) Gate capacitance per unit area
   iii) Gate capacitance. **(06 Marks)**

c. By considering a suitable example, compare the metal interconnect and electro – optical interconnect models. **(08 Marks)**

6 a. Explain the structured design approach for an n – bit bus arbitration logic and draw the NMOS stick diagram for its basic cell. **(10 Marks)**

b. With a suitable example, explain the concept of dynamic CMOS logic. **(10 Marks)**

7 a. What is two phase clocking? Draw and explain a combinational circuit to generate a two phase clock. **(06 Marks)**

b. With a neat diagram and relevant expressions, explain the implementation of a 4 bit ALU, using full adders. **(12 Marks)**

c. What is regularity? Explain. **(02 Marks)**

8 Write short notes on :
a. Super buffers.
b. Barrel shifter.
c. Switch logic. **(20 Marks)**
d. Dynamic shift register.

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