2002 SCHEME

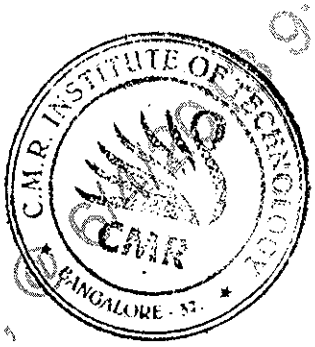
USN | | | | | | | | | | |

CS33

Third Semester B.E. Degree Examination, June/July 2013
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***



1 a. Prove the following:
   i) $\bar{x}y + yz\,\bar{x}\bar{z} = xy + \bar{x}\bar{z}$
   ii) $\bar{x}\bar{y} + \bar{x}z + \bar{x}y + xy = 1$
   iii) $(x + y)(\bar{x}\bar{y} + z)(\overline{\bar{y} + xz}) = \bar{x}y$. **(10 Marks)**

   b. Complement the following Boolean expressions:
   i) $f = \bar{y}(\overline{xz} + xyz)$
   ii) $f = x\bar{z}(\overline{\bar{x}z} + \overline{xy})$. **(05 Marks)**

   c. Implement the following using NAND gates:
   i) $f = x\bar{y} + xz$
   ii) $f = x + \bar{y}z$ **(05 Marks)**

2 a. Using k-map find out SOP expression for
   $f(w, x, y, z) = \sum m(0, 1, 5, 6, 7, 8, 9) + \sum d(10, 11, 12, 13, 14, 15)$. **(10 Marks)**

   b. Using Quine Mcclusky method find out SOP expression for the following function:
   $f(x, y, z) = \sum m(0, 1, 3, 4, 6, 7)$. **(10 Marks)**

3 a. Write complement of the following in disjunctive canonical form
   i) $f(x, y, z) = \sum m(0, 2, 5)$
   ii) $f(x, y, z) = \pi M(1, 2, 5, 7)$
   iii) $f(x, y, z) = \sum m(1, 4, 6)$. **(10 Marks)**

   b. Design full adder to add 2 bits a_i and b_i along with carry c_i and generate and implement sum s_i and carry c_{i+1}. **(10 Marks)**

4 a. Explain the following properties of integrated circuits of SSI type.
   i) Propagation delay
   ii) Noise margin
   iii) Fan-in
   iv) Fan-out.
   and compare TTL and CMOS gates in respect of these properties. **(10 Marks)**

   b. With circuit diagram, explain the operation of CMOS NAND gate and what are the advantages over corresponding TTL gates. **(10 Marks)**

5 a. Realize the function using 8 to 1 MUX treat a, b, c, d as select lines
   $f(a, b, c, d) = \sum m(0, 1, 5, 6, 7, 9, 10, 15)$. **(10 Marks)**

b. Implement the following functions using 3 × 4 × 2 PLA.
$f_1(a, b, c) = \sum m (1, 2, 3, 7)$
$f_2 (a, b, c) = \sum m (1, 5, 7)$. **(10 Marks)**

6 a. With diagram explain universal shift register. **(10 Marks)**
b. Discuss what is race around condition in JK flip flop and describe master-slave JK flip flop with diagram. **(10 Marks)**

7 a. Draw the state diagram of mearly machine whose output is 1 iff the last 3 inputs were 010 assuming that the sequence could overlap. **(10 Marks)**
b. Configure a synchronous 4 bit up-counter with parallel load inputs to count from 0000 to 1001 ie, Mod-10 counter and explain. **(10 Marks)**

8 Write short notes on:
a. Ripple counter
b. PAL
c. Magnitude comparator
d. Decoder. **(20 Marks)**