2002 SCHEME

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CS33

Third Semester B.E. Degree Examination, December 2011
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 Prove that:

a. $\bar{x}\bar{y} + y\bar{z} + \bar{x}z = \bar{x}y + \bar{y}z + x\bar{z}$ **(04 Marks)**

b. If $\bar{w}x + y\bar{z} = o$, then prove that, $wx + \bar{y}(\bar{w}+\bar{Z}) = wx + xz + \bar{x}\bar{z} + \bar{w}\bar{y}Z$ **(05 Marks)**

c. Implement the following function with only four NAND gates. Only the normal inputs are available. $F = \bar{w}xz + \bar{w}yz + \bar{x}y\bar{z} + +wx\bar{y}z$, donteare = wyz. **(06 Marks)**

d. Express the Boolean function, f(x, y, z) = x + $\bar{x}\bar{z}(y + z)$ in minimal canonical sum of products and products of sums expressions. **(05 Marks)**

2 a. Using Karnangh map, determine all minimal sum of products and minimal products for the Boolean function, $f(w, x, y, z) = xz + x\bar{y}\bar{z} + \bar{w}\bar{x}y + wy\bar{z}$. **(06 Marks)**

b. Let $g(w, x, y, z) = \sum m\ (1, 3, 4, 12, 13)$ and $f(w, x, y, z) = \sum m\ (0, 1, 3, 4, 6, 8, 10, 11, 12, 13)$ Determine a minimal sum and a minimal product for the function h(w,x,y,z) such that $g(w, x, y, z) = f(w, x, y, z) \bullet h(w, x, y, z)$. **(08 Marks)**

c. You are supplied with just ONE NOT gate an unlimited amount of diode gates and are required to design a circuit which realizes the expression, $T(w, x, y, z) = \bar{w}x + \bar{x}y + x\bar{z}$. Only unprimed variables are available as inputs. **(06 Marks)**

3 a. Using Quine-McClnskey method, obtain all the prime implements and minimal sum of products for the function, $f(w, x, y, z) = \sum m\ (0, 1, 2, 6, 7, 9, 10, 12) + dc\ (3, 5)$. **(10 Marks)**

b. For the Boolean function given, determine a minimal sum and a minimal product, using variable entered maps, where w,x and y are the map variables.
$f(w, x, y, z) = \sum m\ (1, 5, 6, 7, 9, 11, 12, 13) + dc\ (0, 3, 4)$. **(10 Marks)**

4 a. Describe, how a MOSFET con be sued as a resistor. **(06 Marks)**

b. Explain the functioning of two input CMOS Nand gate, with a truth table. **(08 Marks)**

c. Compare the characteristics of logic families with various parameters, TTL, MOS and CMOS. **(06 Marks)**

5 a. Design an 8 to 3 line encoder and show its logic diagram and operation. **(08 Marks)**

b. Write the structure of programmable read only memory. Implement the functions,
$f_1(x_2, x_1, x_0,) = \sum m\ (0, 1, 2, 5, 7)$
$f_2(x_2, x_1, x_0,) = \sum m\ (1, 2, 4, 6)$ using PROM. **(08 Marks)**

c. Write a note on programmable array logic devices. **(04 Marks)**

6 a. Design and explain the operation of a subtractor, with a logic diagram. **(07 Marks)**

b. Realize the functions $f_1(x_2, x_1, x_0,) = \sum m\ (0,2,4)$
$F_2(x_2, x_1, x_0,) = \sum m\ (1, 2, 4, 5, 7)$, using a decoder circuit. **(05 Marks)**

c. Implement the function $f(w, x, y, z) = \sum m\ (4, 5, 7, 8, 10, 12, 15)$ using 4 to 1 multiplexers and external gates. **(08 Marks)**

7 a. Design a synchronous Mod-6, counter, using clocked J K flip-flops. Draw the complete circuit diagram. **(10 Marks)**

b. Explain the functioning of serial-in, parallel-out unidirectional shift register with a logic diagram and output waveform. **(10 Marks)**

8 a. Design a synchronous counter whose counting sequence is 0,1,4,6,3,5,0,1..... Use JK flip-flops for implementation. **(10 Marks)**

b. How an analysis of clocked synchronous sequential network is performed? Explain with an example. **(10 Marks)**

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