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Third Semester B.E. Degree Examination, June/July 2011
Logic Design

Time: 3 hrs.   Max. Marks:100

Note: *Answer any FIVE full questions.*

1 a. Without first constructing the truth table, prove the following relationships, using the basic Boolean postulates and theorems in the process:

   i) $(x + y)(\bar{x} + y) = xz + \bar{x}\, y$ ii) $(x + y)(\overline{xz} + z)(\overline{y + xz}) = \bar{x}\, y$

   iii) $\overline{(xy + yz + xz)} = \bar{x}\,\bar{y} + \bar{y}\,\bar{z} + \bar{x}\,\bar{z}$ iv) $xy + yz + xz = \overline{xy} + \overline{yz} + \overline{xz}$ **(08 Marks)**

   b. Using Boolean algebra postulates and theorems, simplify each of the following expressions as disjunctive normal formula:

   i) $yz + \bar{x}\,\bar{y}z + xy\bar{z}$ ii) $\bar{x}\,\bar{y}\,\bar{z} + \bar{x}\,\bar{y}z + xy\bar{z} + x\bar{y}\,\bar{z} + \bar{x}yz + xyz$ iii) $\overline{(x + yz)} + \bar{y}z$ **(06 Marks)**

   c. Implement the logical expression $f(w, x, y, z) = \bar{y} + wx + \overline{wxz}$, using only NOR gates. Do not alter the given form of the expression. Assume that independent input variables are available in both complemented and uncomplemented forms.   **(06 Marks)**

2 a. Using Quine-McCluskey method, obtain all the prime implicants of the Boolean function
   $f(w, x, y, z) = \Sigma m\,(0, 1, 2, 6, 7, 9, 10, 12) + dc\,(3,5)$ **(07 Marks)**

   b. Determine minimal sum using variable-entered maps (assuming w, x and y to be map variables) for the function $f(w,x,y,z) = \Sigma m\,(0,3,4,5,8,9,11,12,13)$.   **(07 Marks)**

   c. Design a 3-input, 1-output minimal gate combinational network that produces logic 1 output, when majority of its inputs are logic -1. Otherwise, the network output is to be logic 0.   **(06 Marks)**

3 a. Implement a BCD adder using two 4-bit binary adders (block schematic forms) and an additional logic circuit. Explain with illustration the process of identifying the correct sum out of possible invalid BCD sum resulting during such addition.   **(05 Marks)**

   b. Write the truth table for 4 to 2 lines priority encoder with a valid output, where the highest priority is to higher order bits. Also, workout the logical expressions for the output variables involved in the process.   **(05 Marks)**

   c. Realize the Boolean expressions $f_1(x,y,z) = \Sigma m\,(0,2,6,7)$ and $f_2(x,y,z) = \Sigma m\,(3,5,6,7)$, using NAND gates and an active low 3 to 8 decoder.   **(05 Marks)**

   d. Implement the Boolean expression $f(w,x,y,z) = \Sigma m\,(1,2,6,7,9,11,12,14,15)$ using 8 to 1 line multiplexer, where w, x and y appear on select lines S_2, S_1 and S_0 respectively.   **(05 Marks)**

4 a. An application of PROM is to realize lookup tables for arithmetic functions. Using a PROM of the smallest appropriate size, draw the logic diagram in PLD notation for a PROM realization of the lookup table corresponding to the decimal arithmetic expression $F(X) = 3X + 2$ for $0 \le X \le 7$, where $F(X)$ and X are expressed in binary.   **(10 Marks)**

   b. Realize the following Boolean functions with PLA having provisions for both true and complemented outputs. By considering just the prime implicants of the individual functions, determine the minimum number of product terms needed for realization of f_1 and f_2 in the true form. Draw the logic diagram of the realization in PLD notation and show the corresponding PLA table also.

   $f_1\,(x,y,z) = \Sigma m\,(3,6,7)$ $f_2\,(x,y,z) = \Sigma m\,(0,1,2,6,7)$ **(10 Marks)**

5 a. What is a Flip-Flop? Discuss the SR latch with relevant logic circuit and function table.
(04 Marks)

   b. The input signals shown in Fig.Q5(b) are applied to the SR latch, when initially the latch is in its 0-state. Sketch the Q and $\overline{Q}$ output signals. Assume that all the timing constraints are satisfied.
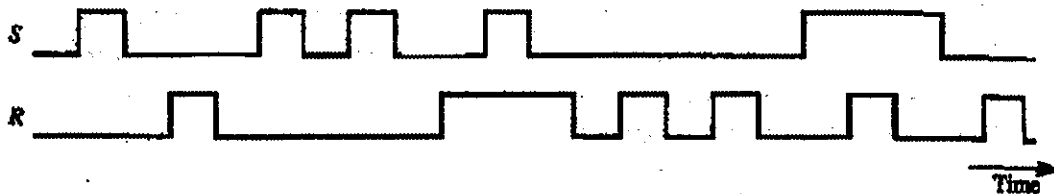(10 Marks)

Fig.Q5(b)

   c. Workout the characteristic equation of a JK Flip-Flop, with relevant truth table and K-map representations.
(06 Marks)

6 a. Explain the properties i) Propagation delay   ii) Fan-in and   iii) Fan-out of logical gate. Discuss their significance with illustrations.
(06 Marks)

   b. Discuss the implementation of a two input NAND gate, using CMOS devices.   (07 Marks)

   c. Write the voltage table for the NMOS circuit shown in Fig.Q6(c), if the inputs take values of VDD or ground. Find the minterm canonical expression of the output.   (07 Marks)
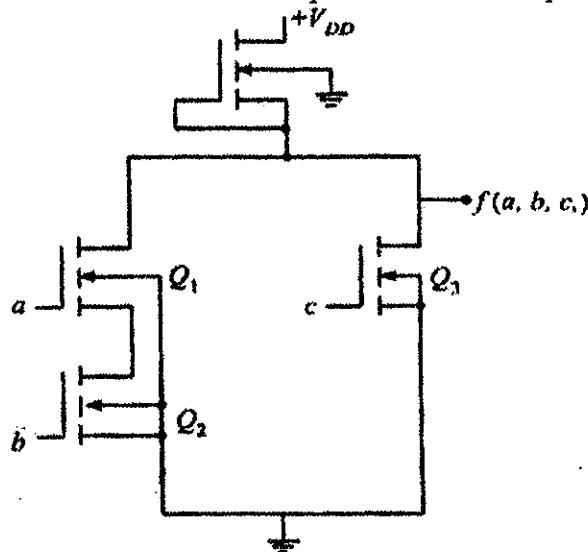

Fig.Q6(c)

7 a. Design a synchronous Mod-6 counter, using clocked JK flip-flops.   (10 Marks)

   b. Obtain a minimal state table for a clocked synchronous sequential network having a single input line x, in which the symbols 0 and 1 are applied and a single output line z. An output of 1 is to be produced coincident with each third multiple of the input symbol 1. At all other times, the network is to produce 0 outputs. An example of input/output sequences that satisfy the conditions of the network specifications is

   x = 0 1 1 0 1 0 1 1 1 0 0 0 1 1 1 0
   y = 0 0 0 0 1 0 0 0 1 0 0 0 0 0 1 0 0
(10 Marks)

8   Write explanatory notes on :

   a. Algorithm for generating prime implicants using Quine-McCluskey method.
   b. High speed addition using Carry look ahead adders.
   c. Serial-in, serial-out & parallel-in, serial-out Shift registers.
   d. Binary ripple counter.
(20 Marks)

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