2002 SCHEME

USN | | | | | | | | | | |

CS33

Third Semester B.E. Degree Examination, June/July 2014
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Express the following Boolean function as sum of minterms and product of max terms
$F(x, y, z) = (xy + z)(xz + y)$. **(04 Marks)**

b. Reduce the expression using appropriate formula
$F = A\left[B + \bar{C}(\overline{A \cdot B + A\bar{C}})\right]$. **(04 Marks)**

c. Define the following, with an example :
i) DOS ii) Canonical SOP iii) Disjunctive canonical form. **(06 Marks)**

d. Prove NOR and NAND gate are an universal gates. **(06 Marks)**

2 a. Reduce the following expression using K–Map and implement it using basic gates :
$F(A, B, C, D) = \pi M(0, 1, 2, 6, 8, 10, 11, 12)$. **(08 Marks)**

b. Reduce the following function using K – MAP technique and identify prime implicates and essential prime implicants.
$F(A, B, C, D) = \sum m(0, 12, 3, 6, 7, 13, 15)$. **(06 Marks)**

c. Obtain the real minimal expression for $F = \sum m(1, 2, 4, 6, 7)$, using K – MAP and implement it using universal gates. **(06 Marks)**

3 a. Obtain the minimal expression for $F = \sum m(1, 3, 13, 15) + \sum d(8, 9, 10, 11)$ using the Quine Mc Clusky method. **(12 Marks)**

b. Simplify the following equation using MEV method :
$F(W, X, Y, Z) = \sum m(2, 4, 5, 10, 11, 14) + \sum d(7, 8, 9, 12, 13, 15)$. **(08 Marks)**

4 a. Explain the TTL with totem – Pole output stage. **(06 Marks)**

b. Explain with the help of circuit diagram the tristate TTL logic. **(08 Marks)**

c. Explain with the help of circuit diagram the working of two input CMOS NOR gate. **(06 Marks)**

5 a. Design two bit binary comparator. **(07 Marks)**

b. Explain the concept of carry look ahead adder. **(07 Marks)**

c. Show have the PLA circuit shown below would be programmed to implement full adder. **(06 Marks)**

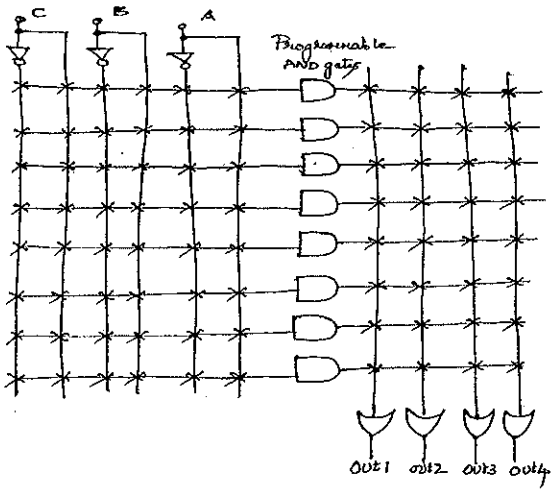

Fig. Q5(c)

6 a. Implement F(w, x, y, z) = $\sum$m(1, 3, 4, 11,12, 13, 14, 15) using 8 : 1 MUX. **(07 Marks)**

b. Bring out the differences between combinational and sequential circuits. **(05 Marks)**

c. Explain Master–Slave JK–FF with the help of timing diagram. **(08 Marks)**

7 a. What are shift registers, explain the different forms of shift registers. **(10 Marks)**

b. Design a synchronous MOD – 6 counter. **(10 Marks)**

8 a. Obtain a reduced state table and reduced state diagram for the sequential machine whose state diagram is shown below : **(08 Marks)**

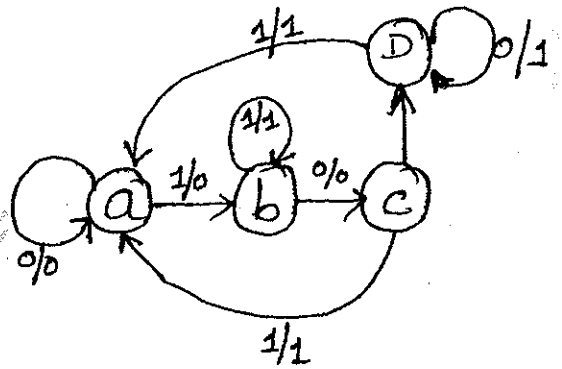

Fig. Q8(a)

b. Bring out the comparison between synchronous sequential circuit and asynchronous sequential. **(06 Marks)**

c. Write a note on the following clocked sequential circuit models :

i) Moore model

ii) Mealy model. **(06 Marks)**

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