CMR
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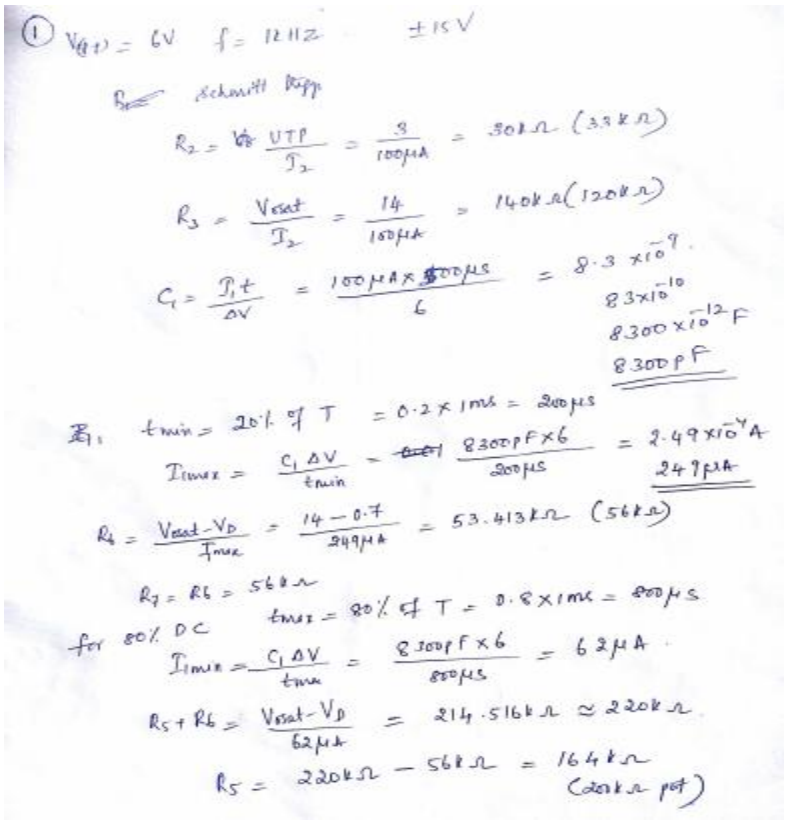
Internal Assesment Test - II

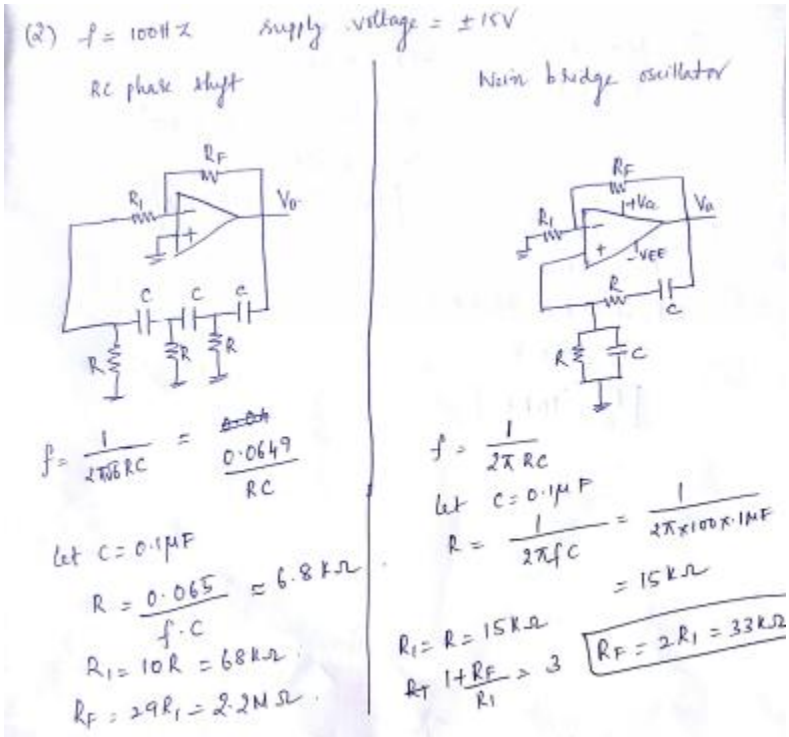
Sub:	**OPERATIONAL AMPLIFIERS AND LINEAR ICs**							Code:	15EE46
Date:	10 / 05/ 2017	Duration:	90 mins	Max Marks:	50	Sem:	IV	Branch:	EEE
Answer Any FIVE FULL Questions									

		Marks	CO	RBT
1	Using an Opamp uA741 IC design a triangular/rectangular signal generator with $V_{o(p-p)}$=6V and frequency 1Khz with ±15V supply. Modify the circuit to provide duty cycle adjustment from 20% to 80%.	[10]	C406.5	L3
2	Design a RC phase shift oscillator and Wein bridge oscillator to generate a sinusoidal output of 100Hz and supply voltage ±15V using any bipolar Opamp.	[10]	C406.5	L2
3	Design a non inverting Schmitt trigger to have UTP=+3V and LTP=-5V using an Op-amp uA741 IC with supply voltage Vcc=±15V.	[10]	C406.4	L3
4	Explain the circuit of a full wave precision rectifier using a half wave rectifier and summing circuit .Demonstrate the input and output waveforms.	[10]	C406.3	L2
5	Demonstrate the operation of peak clipper using Zener diodes and Precision clipper using dead zone circuit with necessary waveforms.	[10]	C406.3	L2
6	Discuss the operation of weighted resistor DAC and R-2R ladder DAC with circuit diagram.	[10]	C406.6	L2
7	Discuss the operation of successive approximation ADC and dual slope ADC with circuit diagram.	[10]	C406.6	L2

1.

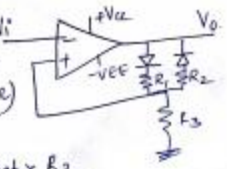

① $V_{(pp)} = 6V$ $f = 1kHz$ $\pm 15V$
Schmitt Trigg
$R_2 = \frac{UTP}{I_2} = \frac{3}{100\mu A} = 30k\Omega$ (33kΩ)
$R_3 = \frac{V_{sat}}{I_2} = \frac{14}{100\mu A} = 140k\Omega$ (120kΩ)
$C_1 = \frac{I_1 t}{\Delta V} = \frac{100\mu A \times 500\mu s}{6} = 8.3 \times 10^{-9}$
8.3×10^{-10}
$8.300 \times 10^{-12} F$
8.300pF
t_{min} = 20% of T = $0.2 \times 1ms = 200\mu s$
$I_{max} = \frac{C_1 \Delta V}{t_{min}} = \frac{8300pF \times 6}{200\mu s} = 2.49 \times 10^{-4} A$
249μA
$R_4 = \frac{V_{sat} - V_D}{I_{max}} = \frac{14 - 0.7}{249\mu A} = 53.413k\Omega$ (56kΩ)
$R_7 = R_6 = 56k\Omega$
for 80% DC t_{max} = 80% of T = $0.8 \times 1ms = 800\mu s$
$I_{max} = \frac{C_1 \Delta V}{t_{max}} = \frac{8300pF \times 6}{800\mu s} = 62\mu A$
$R_5 + R_6 = \frac{V_{sat} - V_D}{62\mu A} = 214.516k\Omega \simeq 220k\Omega$
$R_5 = 220k\Omega - 56k\Omega = 164k\Omega$
(200kΩ pot)

2.


(2) $f = 100Hz$ Supply voltage = $\pm 15V$
RC phase shift
R_F
R_1
V_0
C C C
R R R
$f = \frac{1}{2\sqrt{6}RC} = \frac{0.0649}{RC}$
Let $C = 0.1\mu F$
$R = \frac{0.065}{f \cdot C} \simeq 6.8k\Omega$
$R_1 = 10R = 68k\Omega$
$R_F = 29R_1 = 2.2M\Omega$
Wein bridge oscillator
R_F
$1+V_0$
V_0
R_1
$-V_{EE}$
R C
R C
$f = \frac{1}{2\pi RC}$
Let $C = 0.1\mu F$
$R = \frac{1}{2\pi f C} = \frac{1}{2\pi \times 100 \times 1\mu F}$
$= 15k\Omega$
$R_1 = R = 15k\Omega$
R_T $1 + \frac{R_F}{R_1} > 3$
$R_F = 2R_1 = 33k\Omega$

3.

(3) UTP = +3V LTP = −5V $V_{cc} = \pm 15V$



$R_3 = \frac{UTP}{I_1} = \frac{3}{500\mu A} = 6\times10^{-3}\times10^{6}\,\Omega$

$6k\Omega\,(5.6k\Omega)$

$UTP = \frac{V_{sat} \times R_3}{R_1 + R_3}$ $LTP = \frac{V_{sat} \times R_3}{R_2 + R_3}$

$3 = \frac{14 \times 5.6k\Omega}{R_1 + 5.6k\Omega}$ $3(R_1 + 5.6k\Omega) = 14\times5.6k\Omega$

$3R_1 + 16.8k\Omega = 78.4\times10^{3}$

$3R_1 = 61.6k\Omega$

$\boxed{R_1 = 20.1\Omega\,(18k\Omega)}$

$5 = \frac{14\times5.6k\Omega}{R_2 + 5.6k\Omega}$

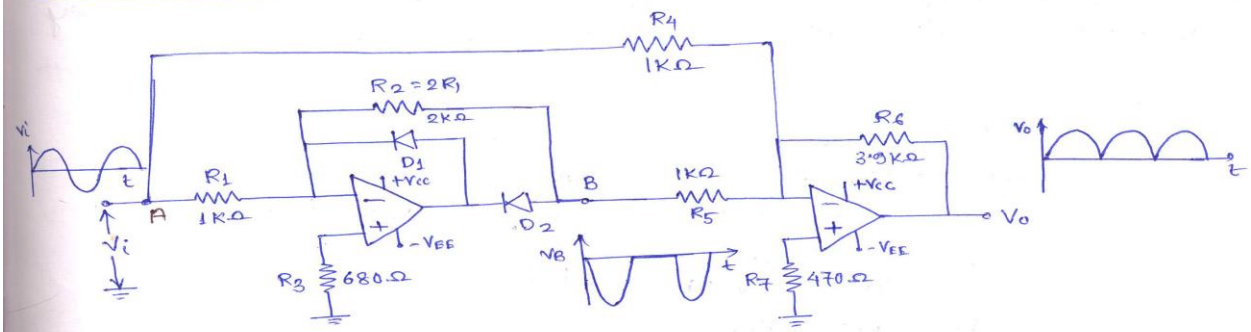
$5R_2 + 28k\Omega = 78.4k\Omega$

$5R_2 = 50.4$

$\boxed{R_2 = 10k\Omega}$

4.

Half-Wave Rectifier and Summing Circuit



The above circuit is a combination of half-wave rectifier with gain = 2 and an inverting adder with gain = 3.9

During +ve half-cycle

Voltage at terminal A = +Vi

While that at terminal B is −2Vi.

[Diode D_1 is off and D_2 is on]

During The output of the summing circuit, with $R_4 = R_5$

$$V_o = -\frac{R_6}{R_4}(V_A + V_B)$$

$$= -\frac{R_6}{R_4}(V_i - 2V_i)$$

$$= -\frac{R_6}{R_4}(-V_i) = \frac{R_6}{R_4} V_i$$

During -ve half-cycle

$V_A = -V_i$

$V_B = 0$ as D_1 is on and D_2 is off.

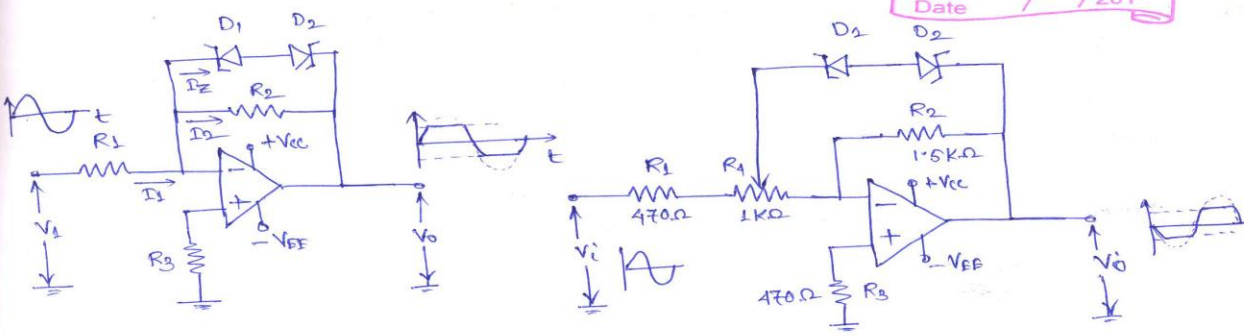
consequently the output is,

$$V_o = -\frac{R_6}{R_4}(V_A + V_B) = -\frac{R_6}{R_4}(-V_i + 0)$$

$$\boxed{V_o = +\frac{R_6}{R_4} V_i}$$

5.

Limiting circuits – Peak clipper



Back to back zener diodes are used to clip-off the peaks of the output voltage waveform. One diode is forward biased and the other diode is in reverse breakdown region when the output voltage is greater than $(V_F + V_Z)$. So, the output voltage can't exceed $\pm(V_F + V_Z)$. As long as the output voltage is less than this limit, the circuit behaves as inverting amplifier, unaffected by the diodes.

The second circuit is a modification of the first circuit where a resistor R_4 is connected in series with R_1. Using R_4 we can change the limiting voltage.

Suppose $R_1 = R_4 = R_2$ and $(V_Z + V_F) = 4V$. With moving the contact at the right side of R_4,

$$V_{o(max)} = V_Z + V_F = \pm 4V \quad \text{——— (1)}$$

With moving the contact at the left of R_4,

$$V_{R2} + V_{R4} = V_Z + V_F = \pm 4V$$

With $R_2 = R_4$, $V_{R2} = V_{R4} = \pm 2V$

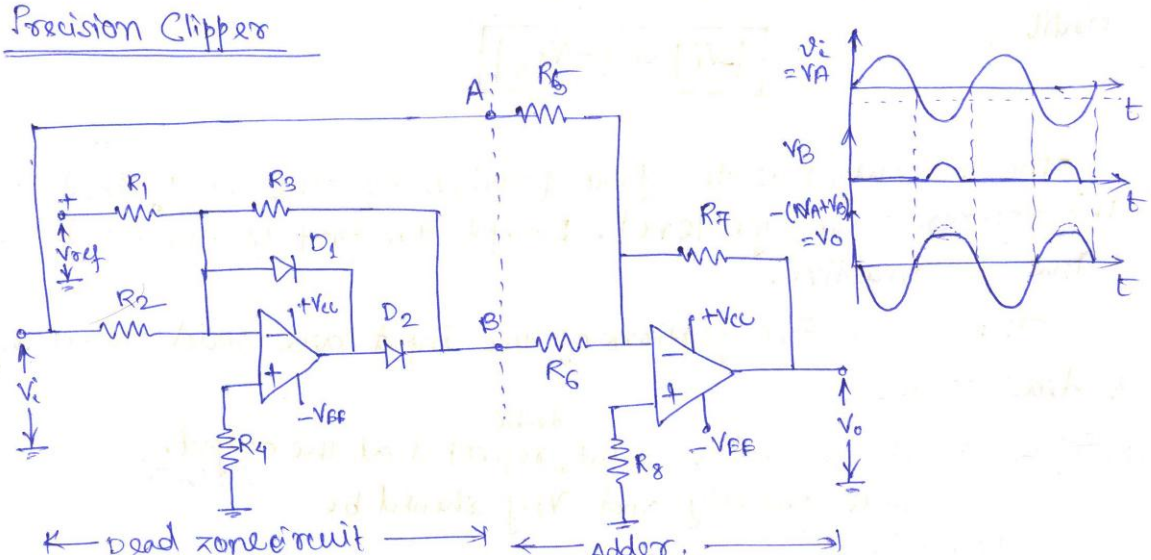
Giving, $\boxed{V_{o(max)} = \pm 2V = V_{R2}}$

This means, by moving the contact the limiting voltage can be changed between ±2 to ±4 volt.

When $R_4 = R_2$, the voltage gain of the circuit, $= -\frac{R_2}{R_1 + R_4}$ until the output limit is reached.

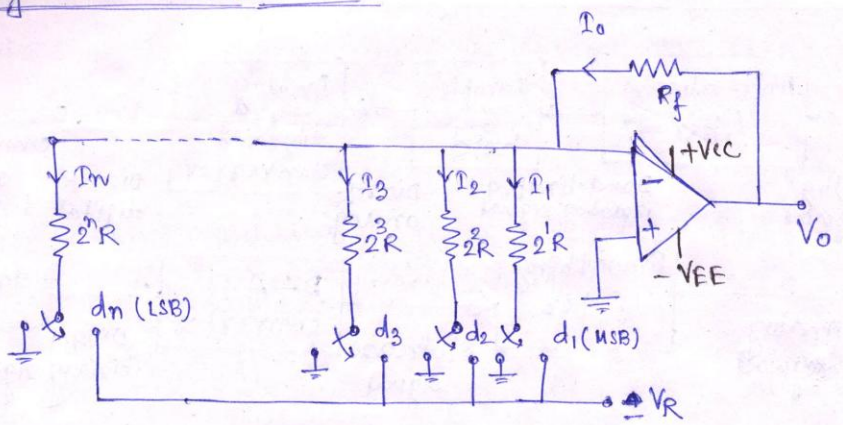
Use: To protect devices that might damage by excessive voltage.

Precision Clipper



6.

Weighted Resistor DAC



The above circuit uses a summing amplifier with binary weighted resistor network. It has n-electronic switches $d_1, d_2, \ldots d_n$ controlled by binary input word. These switches are single pole double through (SPDT) type. The reference voltage is $(-V_R)$.

If, binary input is 'zero', the switch connects the resistor to the ground. If I/p is '1' the switch is connected to $-V_R$.

Applying KCL at the inverting terminal we get,

$$I_0 = I_1 + I_2 + I_3 + \cdots + I_n$$

$$= \frac{V_R}{2R} \cdot d_1 + \frac{V_R}{2^2R} d_2 + \cdots + \frac{V_R}{2^nR} d_n$$

or, $$\frac{V_0}{R_f} = \frac{V_R}{R}\left(\frac{d_1}{2} + \frac{d_2}{2^2} + \cdots + \frac{d_n}{2^n}\right)$$

or, $$\boxed{V_0 = V_R \cdot \frac{R_f}{R}\left(d_1 \cdot 2^{-1} + d_2 \cdot 2^{-2} + \cdots + 2^{-n} d_n\right)}$$

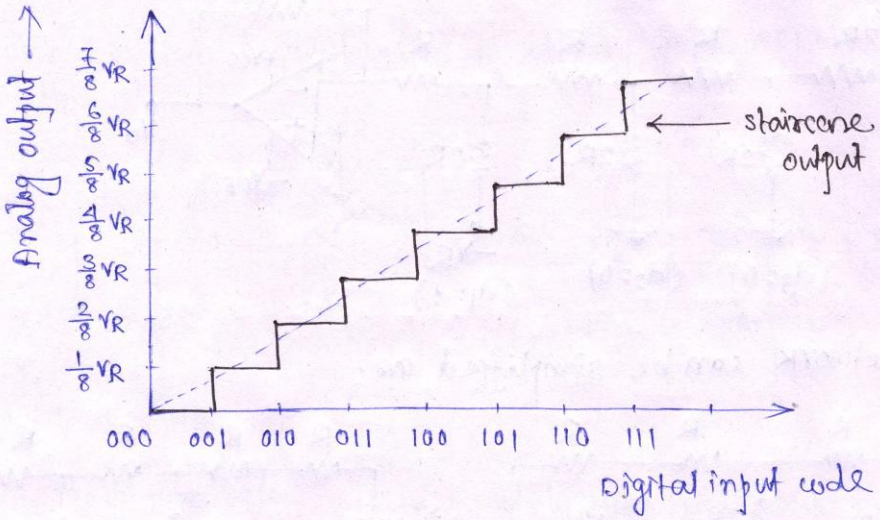
Comparing the above equation with the general expression of DAC we get,

$$V_R = V_{FS}, \quad K = \frac{R_f}{R}$$

If, $R_f = R$ then, $K = 1$, Full scale voltage $(V_{FS}) = V_R$.

$$V_0 = V_R\left(d_1 \cdot 2^{-1} + d_2 \cdot 2^{-2} + \cdots + d_n 2^{-n}\right)$$

The transfer characteristics of a 3-bit DAC is -



R-2R Ladder DAC

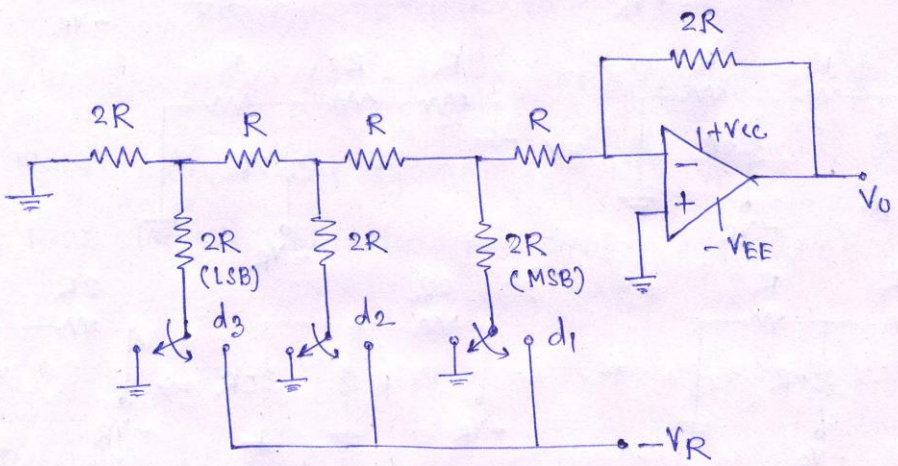


Fig- R-2R Ladder type DAC

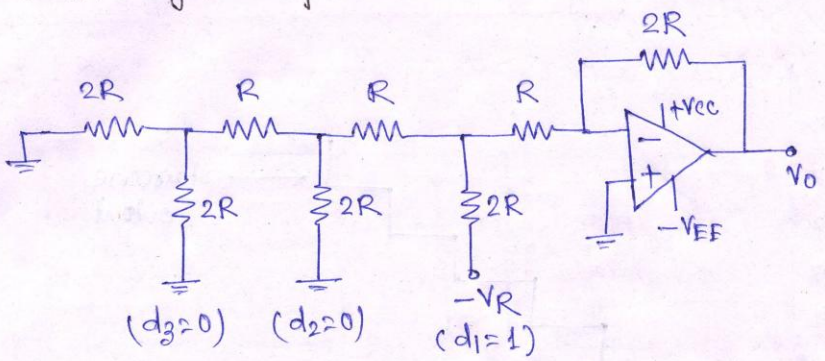
The range for R is 2.5 KΩ to 10 KΩ.

For simplicity, consider a 3-bit DAC. where $d_1 d_2 d_3$ corresponds to the binary word input to the DAC.

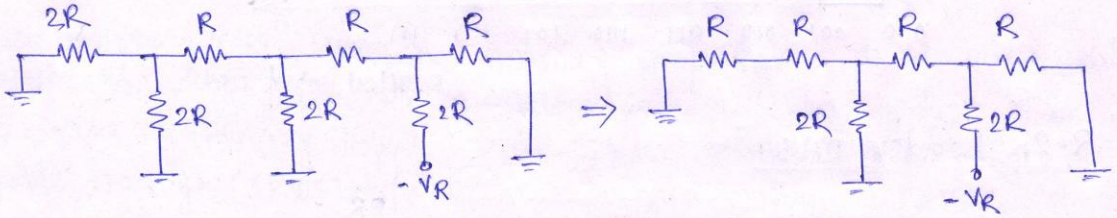
$-V_R$ is the reference voltage.

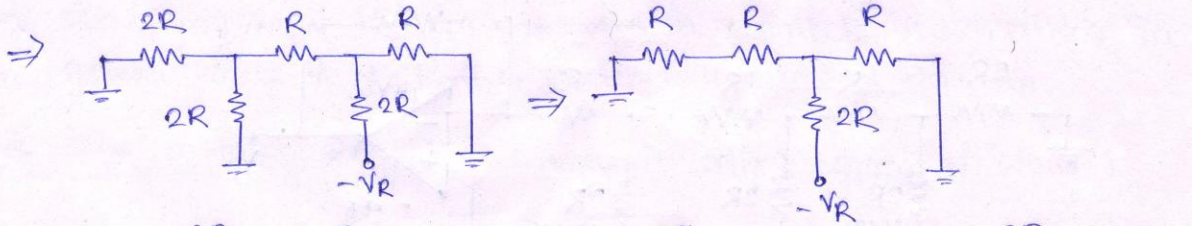
The feedback resistance is 2R. The network consist of R-2R network connected with the op-amp.

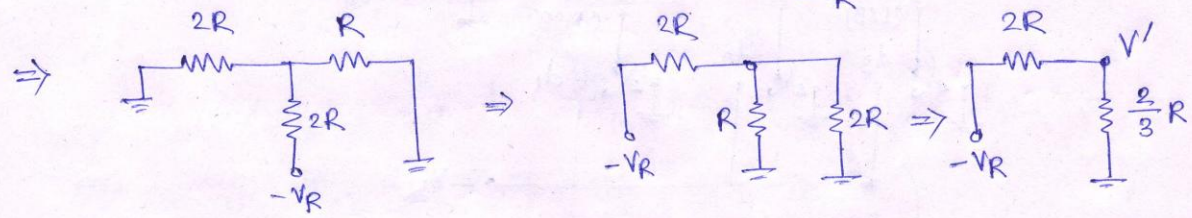
Consider the digital input $d_1d_2d_3 = 100$. The circuit becomes-



The R-2R network can be simplified as-



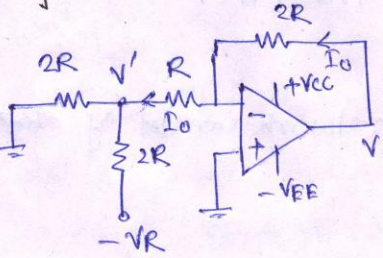




From the simplified circuit,

$$V' = \frac{-V_R \cdot \frac{2}{3}R}{2R + \frac{2}{3}R} = -V_R \cdot \frac{\frac{2}{3}R}{\frac{8}{3}R} = -\frac{V_R}{4}$$

We can represent the circuit as-



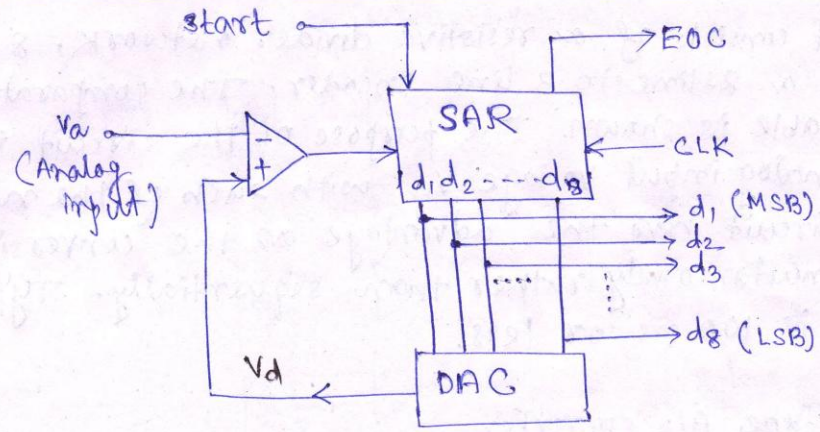
Applying KCL at the inverting terminal

$$\frac{V_o}{2R} = \frac{-V'}{R}$$

or, $\frac{V_o}{2R} = \frac{V_R}{4R}$ or, $\boxed{V_o = \frac{V_R}{2}}$

7.

Successive Approximation Type A/D converter



Functional diagram of the successive approximation ADC.

The conversion sequence for a typical analog input is shown below.

correct digital representation	successive approximation resistor output V_d at different stages in conversion	comparator output
11010100	10000000	1
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

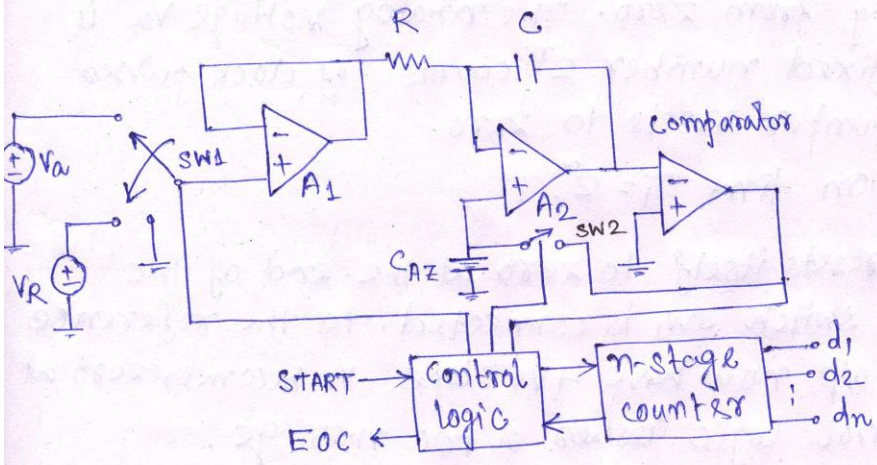
For successive approximation type ADC, for n-bit conversion just n-clock pulses are required. An eight bit converter would require eight clock pulses to obtain a digital output. The circuit uses a successive approximation resistor (SAR) to find the required value of each bit by trial & error.

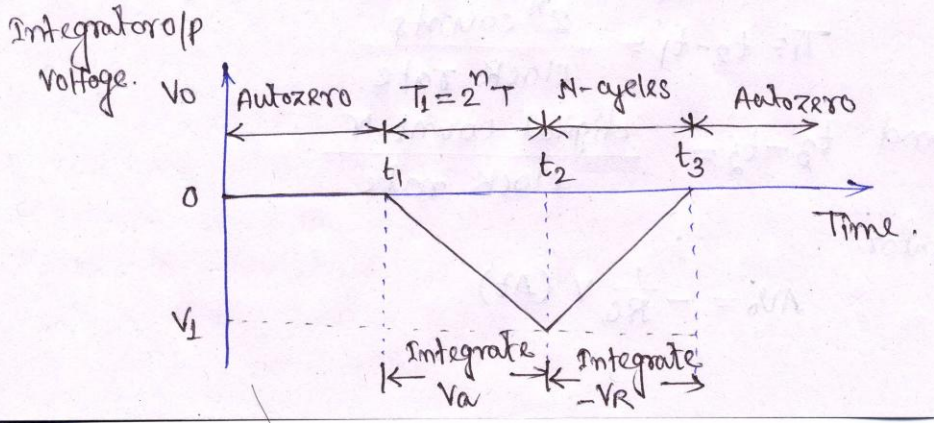
With the arrival of start command, the SAR sets MSB (d_1) = 1 with all other bits to zero, so that the trial code is 10000000 The output Vd of the DAC is now compared with analog input Va. If Va is greater than the DAC output Vd, then, 10000000 is less than the correct representation of the analog input. The MSB is left at '1' and the next lower significant bit is made '1' and further tested.

However if Va is less than the DAC output then 10000000 is greater than the correct digital representation so, reset MSB to '0' and next bit is set to '1' and further tested.

After eight cycles, the EOC command is released and the output of SAR gives the correct digital representation of the

Dual slope ADC





The circuit consists of a high input impedance buffer A_1, precision integrator A_2 and a voltage comparator. The converter first integrates the analog input signal V_a for a fixed duration of 2^n clock period. Then it integrates an internal reference voltage V_R of opposite polarity until the integrator output is zero. The number N of clock cycles required to return the integrator to zero is proportional to the value of V_a averaged over the integration period.

Before the 'start' command arrives, SW1 is connected to GND and SW2 is closed. Any offset voltage present in A_1, A_2 comparator loop after integration, appears across the capacitor C_{AZ} till the threshold of the comparator is achieved.

At the arrival of START command, at $t=t_1$, the control logic opens SW2 and connects SW1 to V_a and enables the counter starting from zero. The analog voltage V_a is integrated for a fixed number 2^n counts of clock pulses after which the counter resets to zero.

Integration time $T_1 = 2^n . T$

The counter resets itself to zero at the end of the interval T_1 and the switch SW_1 is connected to the reference voltage $(-V_R)$. The o/p now have +ve slope. V_o becomes zero at $t=t_3$ and the control logic issues a EOC message.