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14EVE421

Fourth Semester M.Tech. Degree Examination, June/July 2019
Advances in VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain the operation of MESFET under different bias conditions. **(10 Marks)**
b. Determine Pinch off voltage in a MESFET. **(05 Marks)**
c. Bring out the differences between cmos and Bicmos. **(05 Marks)**

2 a. What are the properties of ideal MIS system in equilibrium? Explain energy band diagram for an ideal MIS structure in equilibrium. **(10 Marks)**
b. Calculate the threshold voltage for an 'n' channel MIS device given the following $N_a = 10^{17}cm^{-3}$, $Q_i = 10^{11}$ q/cm^2, d = 20nm and $\phi_{ms} = -0.95V$, $K_i = 3.9$, $n_i = 1.0 \times 10^{10}cm^{-3}$. **(10 Marks)**

3 a. Describe the small signal model for a MOSFET. Obtain the expression for cutoff frequency. **(10 Marks)**
b. Calculate the cutoff frequency of a MOSFET. Given the following information L = 1μm ; n channel device with a p-type substrate ; $\mu_n' = 1200\ cm^2/vs$, z = 10L ; $V_T = 1.1V$; and $V_G = 5V$. **(04 Marks)**
c. Find the maximum width of depletion region for an ideal mos capacitor on p-type silicon in strong inversion given that the doping concentration is $10^{16}cm^{-3}$ and relative dielectric constant is 11.8. Given $n_i = 1.0 \times 10^{10}\ cm^{-3}$. **(06 Marks)**

4 a. What are the important features that arise in short channel MOSFET? Explain any one in detail. **(10 Marks)**
b. Write a note on scaling theory. **(10 Marks)**

5 a. Mention and discuss the advantages of feature of molecular material which can be applied to bio-molecules. **(10 Marks)**
b. With the help of neat diagram, explain the construction and working of carbon nano-tube FET. List out its advantages. **(10 Marks)**

6 a. Derive an expression for the minimum total delay when a series of superbuffers used to drive targe capacitive loads. **(08 Marks)**
b. Explain with circuit diagram the Bicmos implementation of 2 input NAND gate. **(07 Marks)**
c. With the help of truth table, maps and nmos realization, design a pass transistor logic 2 input NAND gate. **(05 Marks)**

7 a. Write down the block diagram, truth table output expression of a 4:1 MUX and its implementation in NOR and NAND modes. **(10 Marks)**
b. Explain 3 input Tally circuit with truth table and stick diagram. **(10 Marks)**

8 a. Discuss structured design technique in detail. **(10 Marks)**
b. Write a note on Full custom design. **(10 Marks)**

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