CBCS SCHEME

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18EVE23

Second Semester M.Tech. Degree Examination, June/July 2019
System Verilog

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the verification process of system verilog. **(10 Marks)**

b. Draw the diagram of layered test bench of system verilog and describe the function of each layer. **(10 Marks)**

OR

2 a. Describe fixed size arrays and dynamic arrays with example. **(08 Marks)**

b. Describe various array methods with examples. **(06 Marks)**

c. Describe typedef and enumerated data types with example. **(06 Marks)**

Module-2

3 a. Describe C-style routine arguments, argument direction, advanced argument types, and default argument values with system verilog program example. **(10 Marks)**

b. Draw the diagram of Testbench-arbiter without interface and write the system verilog code for the arbiter model using ports, testbench using ports, top-level net list without interface. **(10 Marks)**

OR

4 a. Explain tasks, functions and void functions in system verilog. **(06 Marks)**

b. How time values are specified in system verilog, describe with example. **(06 Marks)**

c. Describe testbench-design race condition. Write system verilog code for race condition between testbench and design. **(08 Marks)**

Module-3

5 a. Explain the concept of randomization in system verilog with an example. **(10 Marks)**

b. Describe the solution probabilities in system verilog with example. **(10 Marks)**

OR

6 a. Explain valid constraints and In-line constraints with example. **(10 Marks)**

b. Discuss the common randomization problem with system verilog program. **(05 Marks)**

c. Describe the operation of rand case statement with program. **(05 Marks)**

Module-4

7 a. What are semaphores? Describe semaphore operations by writing system verilog program. **(05 Marks)**

b. Explain the concept of fork...Join, fork....Join_none and fork....Join_any statement. And explain these statements with example. **(10 Marks)**

c. What is an event? Write the program for passing an event into a constructor. **(05 Marks)**

OR

8 a. Write the system verilog code for creating threads in a class with a task that creates the packets. **(08 Marks)**

b. Describe the concept of dynamic thread creation with system verilog code. **(06 Marks)**

c. Describe how single threads and multiple threads are disabled. **(06 Marks)**

Module-5

9 a. What is coverage? Describe different coverage types. **(10 Marks)**

b. What is cross coverage? Write the code for basic cross coverage and give the coverage summary report for basic cross coverage. **(10 Marks)**

OR

10 a. Describe various functional coverage strategies. **(10 Marks)**

b. Describe various coverage options with example. **(10 Marks)**

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