CBCS SCHEME

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18EVE15

First Semester M.Tech. Degree Examination, June/July 2019
Digital VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: *Answer FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Derive the expression for threshold voltage V_T interms of body effect and surface potential. **(10 Marks)**

b. Derive expression for V_{OH}, V_{OL}, V_{IL} and V_{IH} interms of threshold voltage, for n type depletion mode load inverter. **(10 Marks)**

OR

2 a. Calculate the threshold voltage, V_{TO} at $V_{SB} = 0V$, for a polysilicon gate n – channel MOS transistor, with the following parameters : substrate doping density, $N_A = 10^{16}$ cm^{-3}, polysilicon gate density (doping), $N_D = 2 \times 10^{20}$ cm^{-3}. Gate oxide thickness $t_{ox} = 400$ Å, oxide interface fixed charge density, $NO_x = 4 \times 10^{10}$ Cm^{-2} and assume $\phi_{F(gate)} = 0.55V$, E_{si}, the silicon permittivity as $11.7 \times 8.85 \times 10^{-14}$ F/cm and E_{ox}, permittivity of gate oxide in $3.97 \times 8.85 \times 10^{-14}$ F/cm. **(10 Marks)**

b. Explain channel length modulation and substrate Bras effect in MOSFET operation. **(10 Marks)**

Module-2

3 a. Explain 3 stage ring oscillator circuit consisting of identical inverters. **(05 Marks)**

b. Explain RC delay and the Elmore delay models of an interconnect line. **(10 Marks)**

c. Show that switching power dissipation of CMOS inerter is given by $P_{avg} = C_{load} V_{dd}^2 f$, where f is the switching frequency. **(05 Marks)**

OR

4 a. Obtain expression for Z_{PHL} and Z_{PLH} for CMOS inverter interms of V_T and V_{DD} and capacitance. **(10 Marks)**

b. With suitable circuit explain, how to estimate interconnect parasities and capacitance. **(10 Marks)**

Module-3

5 a. Explain Hot electron injection mechanism and Fowler – Nordheim tunneling mechanism in Flash memory. **(08 Marks)**

b. Explain briefly flash memory using NOR cell configuration. **(06 Marks)**

c. Write a short note on FRAM. **(06 Marks)**

OR

6 a. Explain operation of three transistor DRAM cell with pull up and read/write circuitry with help of read and write timing diagrams. **(10 Marks)**

b. Explain the operation full CMOS SRAM cell with neat circuit diagram. **(07 Marks)**

c. Differentiate DRAM and SRAM. **(03 Marks)**

Module-4

7 a. Explain how to overcome threshold voltage drop in integrated circuits using voltage boot strapping technique. **(10 Marks)**

b. Explain briefly with suitable circuit structure of ratioless synchronous dynamic logic. **(05 Marks)**

c. Explain the static behaviour of BICMOS inverter. **(05 Marks)**

OR

8 a. Briefly explain cascading problem in dynamic CMOS logic. **(08 Marks)**

b. Explain NP – Domino logic circuit or NORA CMOS logic for high performance dynamic CMOS circuits. **(06 Marks)**

c. Explain the Ebers – Moll equivalent circuit diagram of the npn BJT operating in the Forward active mode. **(06 Marks)**

Module-5

9 a. Explain ESD protection in human body model, machine model and charged device model. **(08 Marks)**

b. Explain parametric yield and performance variability in design for manufacturability. **(06 Marks)**

c. Explain circuit diagram of a pierce crystal oscillator circuit in onchip clock generation and distribution. **(06 Marks)**

OR

10 a. Explain the causes for latch up and guidelines for avoiding latch up. **(10 Marks)**

b. Explain ESD protection in input and output circuits. **(10 Marks)**

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