CBCS SCHEME

USN | | | | | | | | | | |

18EVE251

Second Semester M.Tech. Degree Examination, June/July 2019
Low Power VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the needs of Low Power VLSI Design. **(05 Marks)**

b. Explain the importance of Monte Carlo – simulation technique. **(05 Marks)**

c. Explain the Basic principles of Low Power Design. **(10 Marks)**

OR

2 a. How do we analyse the data correlation in DSP systems? What are the effects of data correlation on bit switching frequency? **(10 Marks)**

b. Explain SPICE power analysis is SPICE Circuit Simulation. **(10 Marks)**

Module-2

3 a. Define static probability. Derive the equation that relates the static probability 'P' of memoryless random logic signal to its expected frequency 'f'. **(10 Marks)**

b. What is entropy? Discuss the power estimation of combinational logic using entropy. **(10 Marks)**

OR

4 a. Write a note on low power digital cell Library. **(10 Marks)**

b. Explain briefly transistor sizing for Leakage Power Reduction. **(10 Marks)**

Module-3

5 a. What is gate re-organization? Explain. **(10 Marks)**

b. Explain the concept BUS invert encoding to achieve low power consumption with relevant equations. **(10 Marks)**

OR

6 a. Define Zero skew and Tolerable skew. Explain the concept of tolerable skew in a typical synchronous system with a pipelined or parallel architecture. Identify two cases of clock skew resulting into proper tolerable skew. **(10 Marks)**

b. Differentiate between single driver scheme and distributed scheme. Explain the concept of buffer insertion in clock tree. **(10 Marks)**

Module-4

7 a. Briefly outline the principle of the following switching activity techniques:
(i) Guarded Evaluation (ii) Bus multiplexing **(10 Marks)**

b. Explain flow graph transformation with operator reduction and control data flow graph and its mapping to hardware architecture. **(10 Marks)**

OR

8 a. With a neat diagram, explain the working of a 8-bit Wallace Tree Multiplier. **(10 Marks)**

b. Explain the concept of worst case delay for Newton-Raphson division. **(10 Marks)**

Module-5

9 a. Explain the sources of power dissipation in DRAM and SRAM. **(10 Marks)**

b. For low power CAD framework, explain the design flow with supporting tools. **(10 Marks)**

OR

10 a. Explain capacitance models for hardware modules and activity models for control signals with respect to architectural estimation. **(10 Marks)**

b. Explain the four phases of operations in a four phase adiabatic logic inverter. **(10 Marks)**

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