CBCS SCHEME

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18EVE21

Second Semester M.Tech. Degree Examination, June/July 2019
Design of Analog and Mixed Mode VLSI Circuits

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

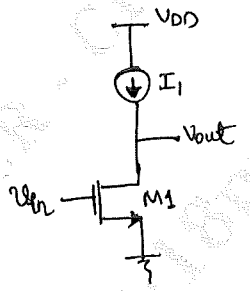
Module-1

1 a. Explain the small signal of a MOSFET including channel length modulation and body effect. Derive the expressions for output resistance 'r_0' and trans conductance due to body effect 'g_{mb}'. **(08 Marks)**

b. Derive the expression for voltage gain of a common source amplifier with resistive load by i) Analytical method ii) Small signal model. **(08 Marks)**

c. In Fig.Q.1(c), M_1 is in saturation. Give the expression for small signal voltage gain of the circuit. **(04 Marks)**

Fig.Q.1(c)



OR

2 a. Explain the second order effects that appear in MOSFET in detail. How these affect drain current? **(10 Marks)**

b. Derive the expressions for voltage gain of a common source stage with source degeneration in presence of body effect and channel length modulation. **(10 Marks)**

Module-2

3 a. Derive the expression of small signal gain of source follower using
i) Analytical method ii) Small signal model. **(10 Marks)**

b. Why non linearity is seen in source followers with NMOS? How this is eliminated? **(04 Marks)**

c. For the circuit shown in Fig.Q.3(c)(i), $(W/L)_1 = 20/0.5$, $I_1 = 200\mu A$, $V_{THO} = 0.6V$, $2\phi_F = 0.7V$, $\mu_n C_{ox} = 50\mu A/V^2$ and $\gamma = 0.4V^2$
Calculate V_{out} for $V_{in} = 1.2V$
If I_1 is implemented as M2 in Fig.Q.3(c)(ii), find the minimum value of $(W/L)_2$ for which M2 remains saturated. **(06 Marks)**

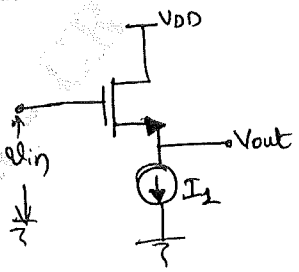


Fig.Q.3(c)(i)

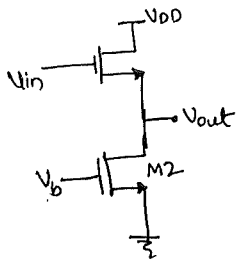


Fig.Q.3(c)(ii)

OR

4 a. Show that small signal gain of a common gate configuration is $A_v = gm\ (1 + \eta)R_D$. **(10 Marks)**

b. With relevant circuit diagram and equations, explain the working of 'Gilbert Cell'. Mention its merits and demerits. **(10 Marks)**

Module-3

5 a. Explain the basic current mirror with relevant equations. Also explain how the effect of channel length modulation is eliminated? **(10 Marks)**

b. What are active current mirrors? Derive the expression for A_v for a differential pair with current source load along with equivalent circuit for calculation of G_m and R_{out}. **(10 Marks)**

OR

6 a. Explain the operation and advantages of a 2 stage op-amp with neat circuit diagram. **(10 Marks)**

b. Compare single stage op-amp topology with 2 stage op-amp. **(10 Marks)**

Module-4

7 a. Explain slew rate and how do we optimize slew rate in op-amp design. **(10 Marks)**

b. Calculate the low frequency PSRR of the feedback circuitry shown in Fig.Q.7(b). **(10 Marks)**

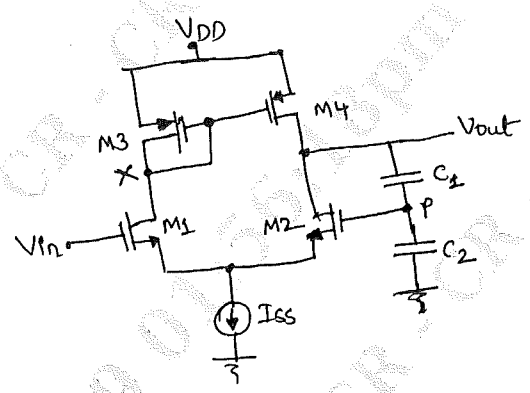


Fig.Q.7(b)

OR

8 a. Explain the operation of a simple charge pump PLL along with its dynamics. **(10 Marks)**

b. Explain the different non-ideal effects in PLL. **(10 Marks)**

Module-5

9 a. Explain the operation of current steering DAC architecture with neat diagrams and equations. **(10 Marks)**

b. Explain the operation of pipeline ADC architecture with neat diagrams and example. **(10 Marks)**

OR

10 a. Explain the operation of charge scaling DAC architecture and derive the expression for output voltage. **(10 Marks)**

b. Explain the operation of successive approximation ADC with an architecture and example showing conversion steps. **(10 Marks)**

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