CBCS SCHEME

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18EVE12

First Semester M.Tech. Degree Examination, Dec.2019/Jan.2020
ASIC Design

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain the following in brief with relevant diagram.
i) Standard cell based ASICs
ii) Gate array based ASIC (channeled, channel less and structured gets array). **(10 Marks)**
b. Explain in detail the steps involved in ASIC design. **(10 Marks)**

OR

2 a. Explain the functioning and limitation of conventional Ripple Carry Adder [RCA], with relevant logic equations and cell diagram. **(10 Marks)**
b. Explain Wallace tree multiplier. **(10 Marks)**

Module-2

3 a. Show that $\hat{D} = NF^{1/N} + P + Q$. **(10 Marks)**
b. Calculate the optimal stage effort and size of transistor for the circuit shown below in Fig.Q3(b). **(10 Marks)**

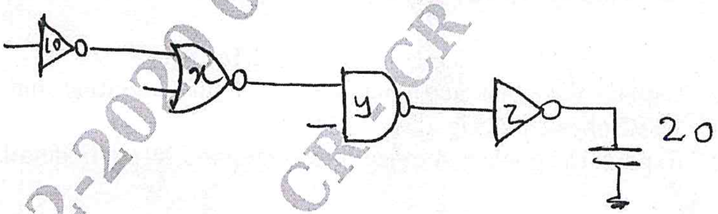

Fig.Q3(b)

OR

4 a. Explain the ACT1 logic module with the help of Shannon's expansion theorem. **(10 Marks)**
b. Explain the Xilinx XC3000 CLB with relevant diagram. **(10 Marks)**

Module-3

5 a. Explain hierarchical design with suitable example. **(10 Marks)**
b. Explain vectored instances and buses for 16-bit D–latch and draw the diagram for 4-bit D–latch with cardinalities. **(10 Marks)**

OR

6 a. List steps in ASIC physical design and describe goals and objective of each step. **(05 Marks)**

b. With relevant equations, explain KL algorithm. Construct the connectivity matrix for the network shown in the below Fig.Q6(b). Also find the gain in the network graph shown if :

i) Nodes 1 and 6 are swapped

ii) Nodes 2 and 8 are swapped. **(15 Marks)**

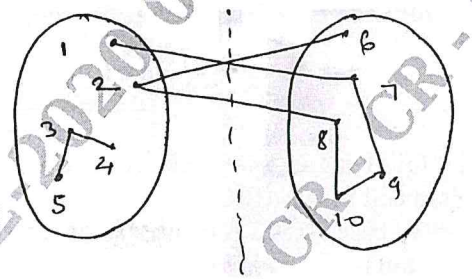

Fig.Q6(b)

Module-4

7 a. Explain the following :

i) Power planning

ii) Clock planning. **(10 Marks)**

b. Explain the concept of measurement of delay in floor planning. **(10 Marks)**

OR

8 a. Write an algorithm for iterative placement improvement method and explain briefly. **(10 Marks)**

b. Explain the following :

i) Placement using simulated annealing

ii) Timing driven placement method. **(10 Marks)**

Module-5

9 a. Explain the goals and objectives of detailed routing and explain the routing method in an ASIC physical design. **(10 Marks)**

b. Explain the goals and objectives of global routing in detail. **(10 Marks)**

OR

10 a. Explain the following :

i) Left edge algorithm

ii) Area–routing algorithm. **(10 Marks)**

b. Explain the following special routing techniques.

i) Clock routing

ii) Power routing. **(10 Marks)**

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