CBCS SCHEME

USN | | | | | | | | | | |

18EVE14

First Semester M.Tech. Degree Examination, Dec.2019/Jan.2020
VLSI Testing

Time: 3 hrs. Max. Marks: 100

Note: ***Answer FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain breaks and transistor stuck – ON fault in CMOS with example. **(10 Marks)**

b. Explain various types of bridging fault with example. **(10 Marks)**

OR

2 a. What is temporary fault? Write state diagram of Markov model with explanation. **(05 Marks)**

b. Explain simulation process with block diagram. **(05 Marks)**

c. Explain the various types of simulators. **(10 Marks)**

Module-2

3 a. For Fig Q3(a), using Boolean difference technique :

i) Detect s-a-0 and s-a-1 on g

ii) Determine partial Boolean difference for y-ℓ-n-f

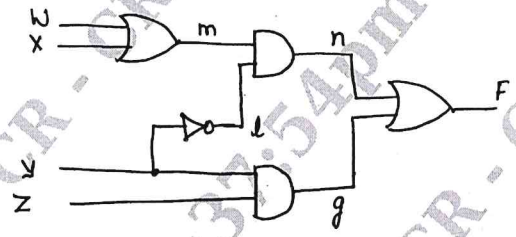

Fig Q3(a) **(06 Marks)**

b. Using Reed – Muller Expansion technique, find test sets for function, F = WX + WY + XY and implement the design. **(08 Marks)**

c. Explain Three – Level OR – AND – OR design with example. **(06 Marks)**

OR

4 a. Find test pattern for line 6 s-a-0, using D – algorithm for Fig Q4(a).

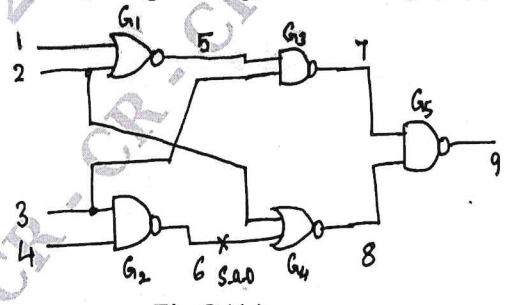

Fig Q4(a) **(10 Marks)**

b. Define PODEM. Explain the working of PODEM. **(05 Marks)**

c. What is the significance of FAN with respect to PODEM? Explain FAN concept with example. **(05 Marks)**

Module-3

5 a. List and explain various possible faults in PLA. Write PLA design for $f_1 = x_1x_2 + x_1'x_2'$ and $f_2 = \overline{x}_1x_2$. **(10 Marks)**

b. What is redundancy? Explain the concept and classification of redundancy with example. **(10 Marks)**

OR

6 a. For a given state table shown in Table Q6(a), find

i) Response for 010 condition
ii) Homing sequence
iii) Distinguishing sequence

Present state	Input/NS	
	X = 0	X = 1
A	B, 0	D, 0
B	A, 0	B, 0
C	D, 1	A, 0
D	D, 1	C, 0

Table Q6(a) **(10 Marks)**

b. Explain the various phases involved in checking experiment based on sequential circuit structure. **(05 Marks)**

c. What is synchronizing sequence? Find synchronizing sequence for Table Q6(c)

Present state	Input/NS	
	X = 0	X = 1
A	B, 1	C, 0
B	A, 0	D, 1
C	B, 0	A, 0
D	C, 1	A, 1

Table Q6(c) **(05 Marks)**

Module-4

7 a. Define controllability and observability with respect to sequential circuit testing. Explain with example circuit. **(08 Marks)**

b. With diagram, explain the working of crosscheck and cross check grid. **(06 Marks)**

c. Explain Boundary scan architecture. **(06 Marks)**

OR

8 a. Explain clocked Hazard free latches in LSSD. **(10 Marks)**

b. Illustrate the significance of partial scan. Design partial scan for a combinational logic. **(10 Marks)**

Module-5

9 a. Explain Pseudo – Random pattern Generator for BIST with example. **(10 Marks)**

b. List and explain various types of output response analysis. **(10 Marks)**

OR

10 a. Explain various test algorithms for RAM. **(10 Marks)**

b. Explain BIST structure for SRAM. **(10 Marks)**

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