

CBCS SCHEME

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18EVE15

First Semester M.Tech. Degree Examination, Dec.2019/Jan.2020 Digital VLSI Design

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- Describe the behavior of MOS system under external bias with energy band diagram and relevant equations. (10 Marks)
 - Explain the channel length modulation with I_{ds} equation. (06 Marks)
 - Write the difference between enhancement mode and depletion mode MOSFET. (04 Marks)

OR

- Explain the effects of short channel in MOS transistor and derive the expression for the same. (08 Marks)
 - Consider a resistive load inverter with $V_{DD} = 5V$, $K'_n = 20 \mu_n / V^2$, $V_{TO} = 0.8V$, $R_L = 200 K\Omega$ and $\frac{\omega}{L} = 2$. Find the critical voltages V_{OL} , V_{OH} , V_{IL} and V_{IH} and find the noise margin of the circuit. (06 Marks)
 - Draw a depletion load nMOS inverter circuit and calculate V_{OH} and V_{OL} of the circuit. (06 Marks)

Module-2

- Draw the neat circuit diagram of CMOS inverter and explain the circuit operation with its characteristics mentioning all five regions. (10 Marks)
 - Consider a CMOS inverter circuit with the following parameters: $V_{DD} = 3.3V$, $V_{TO,n} = 0.6V$, $V_{TO,p} = -0.7V$, $K_n = 200 \mu A/V^2$, $K_p = 80 \mu A/V^2$. Calculate the noise margins of the circuit. (05 Marks)
 - Derive relationship between $\left(\frac{\omega}{L}\right)_p$ and $\left(\frac{\omega}{L}\right)_n$ for symmetric CMOS inverter. Also discuss the effects of K_R variation on VTC. (05 Marks)

OR

- Explain CMOS ring oscillator circuit. What is the expression for frequency in arbitrary odd (n) of cascade connected inverters. (10 Marks)
 - Define propagation delays and derive the expression for T_{pHL} and T_{pLH} for CMOS inverter, using differential equation method. (10 Marks)

Module-3

- Explain four transistor, three transistor, two transistor and one transistor DRAM cell. (10 Marks)
 - Explain memory structure SRAM with read and write circuitry with aid of read and write circuit diagrams. (10 Marks)

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

OR

- 6 a. Explain the memory structure of ferroelectric random access memory. (08 Marks)
 b. Design 4×4 NOR base ROM array that can store the following data given,
 Note : $R_1, R_2, R_3, R_4 \rightarrow$ Address

$C_1, C_2, C_3, C_4 \rightarrow$ Memory locations

R_1	R_2	R_3	R_4	C_1	C_2	C_3	C_4
1	0	0	0	0	1	0	1
0	1	0	0	0	0	1	1
0	0	1	0	1	0	0	1
0	0	0	1	0	1	1	0

- c. Differentiate between DRAM and SRAM.

(08 Marks)
(04 Marks)

Module-4

- 7 a. Explain how to overcome threshold voltage drop in digital circuits using boot strapping technique. (10 Marks)
 b. What is dynamic CMOS logic? Explain with an example. (05 Marks)
 c. Explain briefly with suitable circuit pass transistor in dynamic CMOS logic. (05 Marks)

OR

- 8 a. Explain the static behavior of BiCMOS inverter. (08 Marks)
 b. What is BiCMOS logic circuit? Write an application for it. (04 Marks)
 c. Implement the following function using, BiCMOS logic $Y = \overline{AB + CD}$. (08 Marks)

Module-5

- 9 a. What are the different models of ESD? Explain them with suitable diagrams. (10 Marks)
 b. Draw the circuit diagram to reduce $L \frac{di}{dt}$ noise and write a few lines about their working.

(10 Marks)

OR

- 10 a. Explain factorial design for $n = 3$. (10 Marks)
 b. Explain performance variability minimization and performance modeling. (10 Marks)
