CBCS SCHEME

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18EVE31

Third Semester M.Tech. Degree Examination, Dec.2019/Jan.2020
CAD for Digital Systems

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. What are the important design entities in VLSI design? Explain. **(08 Marks)**

b. Discuss the domains and their hierarchies in VLSI design with Y chart. **(08 Marks)**

c. Enumerate and explain the VLSI design methods and technologies. **(04 Marks)**

OR

2 a. Draw the Y chart showing the VLSI design tools and explain them in detail. **(05 Marks)**

b. How is the correctness of design in checked in prefabrication stage? Explain the methods. **(05 Marks)**

c. Write the pseudo-code description of Dijkstra's shortest path algorithm. Illustrate the evolution of distance attributes when applied to the graph shown in Fig.Q2(c).

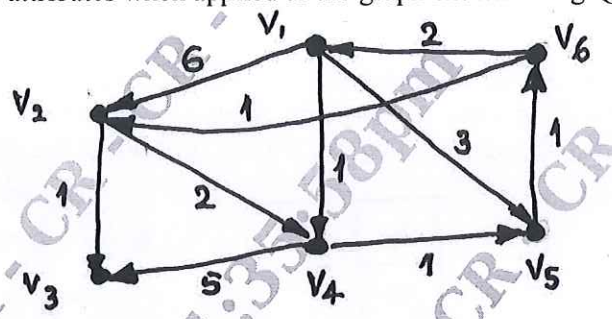


Fig.Q2(c) **(10 Marks)**

Module-2

3 a. Calculate the least cost solution for the travelling salesman problem shown in Fig.Q3(a) using branch and bound algorithm. Show the least-cost path. Draw the search-tree and explain.

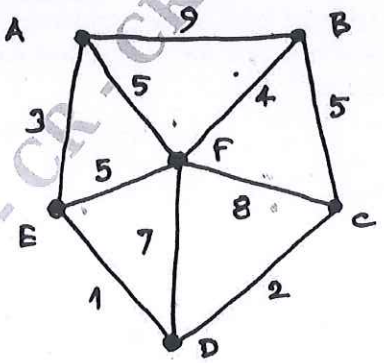


Fig.Q3(a) **(10 Marks)**

b. Write and explain the pseudo-code for simulated annealing. Detail the application in VLSI design with pros and cons. **(10 Marks)**

OR

4 a. Describe briefly VLSI design problem formulation with respect to compaction, informal and graph theoretical formulation and maximum distance constraints with diagrams. **(10 Marks)**

b. Explain the applications of the Bellman-Ford algorithm with pseudo code to the directed graph shown in Fig.Q4(b).

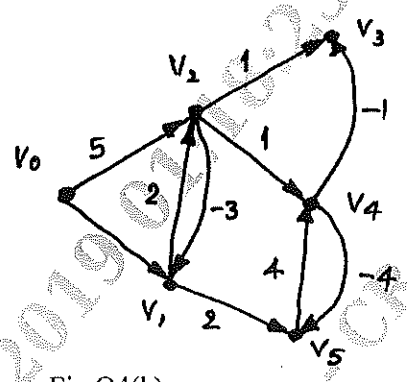


Fig.Q4(b) **(10 Marks)**

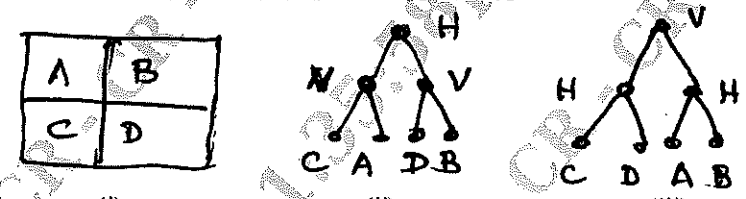
Module-3

5 a. Draw the representations of R.S latch in various graphical models and explain their relevance. **(10 Marks)**

b. Explain wire length estimation metrics with necessary definitions in each case. **(10 Marks)**

OR

6 a. Consider the floor plan shown with inset cells A, B, C, D. A = 2 × 2, B = 1 × 3, C = 1 × 4, D = 2 × 4. Give the shape functions of these cells. Compute the optimal shape of the circuit using slicing tree using tree (ii) and (iii). [Refer Fig.Q6(a)]



(i) (ii) (iii)

Fig.Q6(a) **(10 Marks)**

b. Explain the optimization problems in floor planning. **(10 Marks)**

Module-4

7 a. Discuss the types of local routing problems in detail. **(08 Marks)**

b. Explain Steiner heuristic for Steiner tree construction for the example shown in Fig.Q7(b). Show the Hannan points.

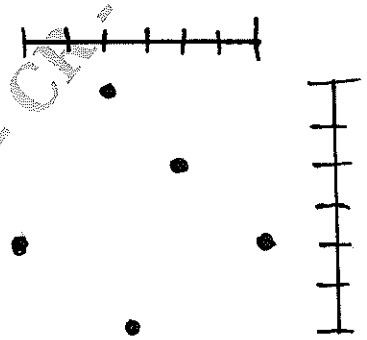


Fig.Q7(b) **(12 Marks)**

OR

8 a. Explain briefly important abstraction levels and the software modules in simulation. **(10 Marks)**

b. Show the switch level modeling with 5 strength values for Static CMOS NAND Gate, nMOS NAND gate and NMOS gate in CMOS domino logic. Explain the reasons for the values attributed. **(10 Marks)**

Module-5

9 a. Write the heuristic to compute the clique partitions of the graph shown in Fig.Q9(a) and draw the cliques in successive steps.

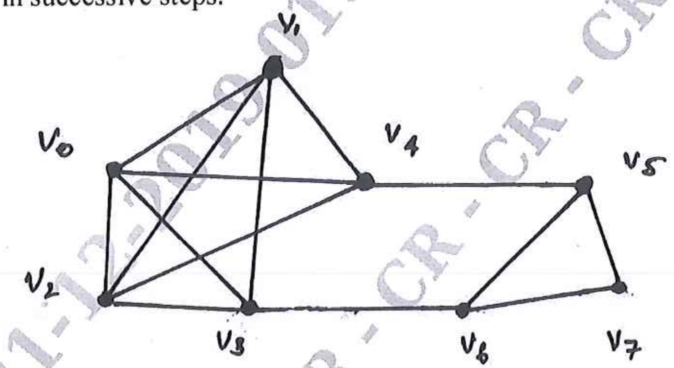


Fig.Q9(a) **(10 Marks)**

b. Write the steps of ROBDD – build algorithm for the function $f = \overline{x}_1.x_3 + \overline{x}_2 \cdot x_3 + x_1x_2$ and the corresponding tree. **(10 Marks)**

OR

10 a. Draw the DFG for the program $x = a * b$, $y = c + d$, $z = x + y$ and different stages of its execution and explain the steps. **(10 Marks)**

b. Draw and explain the most serial and most parallel DFGs for an 8 operand addition $f = a + b + c + d + e + f + g + h$. **(05 Marks)**

c. Draw two different DFGs of the program fragment

if (a > b)
    c ← a – b
else
    c ← b – a

and explain the procedure. **(05 Marks)**

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