

CBCS Scheme

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16ELD41

Fourth Semester M.Tech. Degree Examination, June/July 2018 Synthesis and Optimization of Digital Circuits

Time: 3 hrs.

Max. Marks: 80

Note: Answer FIVE full questions, choosing one full question from each module.

Module-1

- 1 a. Pictorially show the four stages or phases of creating a microelectronic chip. Explain the initial stage in detail. (10 Marks)
- b. Discuss about 'Optimization'. Identify the PARETO points on a design space for FOUR implementation of a logic function $x = pqrs$. (06 Marks)

OR

- 2 a. Draw the data-flow graph and sequencing graph for the following set of computations:

$$x_1 = x + dx;$$

$$u_1 = u - (3 * x * u * dx) - (3 * y * dx);$$

$$y_1 = y + u * dx;$$

$$c = x_1 < a$$
 (06 Marks)
- b. Design a 1-bit full adder in structural VHDL verilog incorporating the half adder model. Include the interface description. (10 Marks)

Module-2

- 3 a. Define : (i) Clique number (ii) Clique cover number (iii) Stability number and (iv) Chromatic number
Determine whether the graph shown in Fig. Q3 (a) is a perfect graph or not using above parameters. (05 Marks)

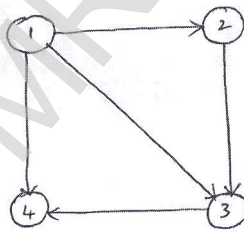


Fig. Q3 (a)

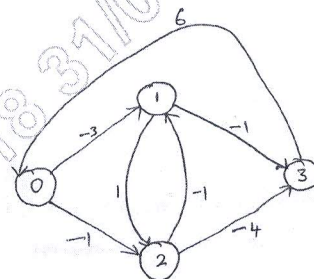


Fig. Q3 (b)

- b. Write the Bellman – Ford algorithm to find the shortest paths. Determine shortest paths for the graph given in Fig. Q3 (b), with the given initial shortest paths, $S'_0 = 0$; $S'_1 = -3$; $S'_2 = -1$; $S'_3 = \infty$. (11 Marks)

OR

- 4 a. Discuss architectural synthesis and optimization problems for,
 - (i) Scheduling in temporal domain. (ii) Binding in spatial domain.
 using the example of differential equation integrator of question 2 (a). (10 Marks)
- b. Analyze the area and performance estimation for,
 - (i) Registers (ii) Steering logic
 - (iii) Wiring and (iv) Control unit of general circuits. (06 Marks)

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Module-3

- 5 a. For a 3-input, 2-output function, $f = \begin{bmatrix} f_1 \\ f_2 \end{bmatrix}$ where $f_1 = \overline{abc} + \overline{a}bc + a\overline{bc} + abc + a\overline{bc}$ and

$f_2 = \overline{abc} + abc$. Determine the

- (i) Minimum cover
- (ii) Irredundant cover and
- (iii) Minimal cover

Represent the covers in 3-D cube notation. (06 Marks)

- b. Use Quine-McClusky method to determine prime implicants, reduced prime implicant table and hence list four possible covers with minimum cardinality for the following function,

$$\sum f = \{0, 2, 4, 5, 6, 7, 8, 9, 10, 11, 13\}$$

Use Expand, Reshape, Reduce and Irredundant operations of Heuristic logic minimization for the obtained prime implicants. (10 Marks)

OR

- 6 a. Perform following transformations:

- | | | |
|-------------------------|--------------------|------------------|
| (i) Elimination | (ii) Decomposition | (iii) Extraction |
| (iv) Simplification and | (v) Substitution | |

for a logic network described by the following equations,

$$p = ce + de$$

$$q = a + b$$

$$r = p + \overline{a}$$

$$s = r + \overline{b}$$

$$t = ac + ad + bc + bd + e$$

$$u = \overline{q}c + q\overline{c} + qc$$

$$v = \overline{ad} + bd + \overline{cd} + a\overline{e}$$

$$w = v$$

$$x = s$$

$$y = t$$

$$z = u$$

(10 Marks)

- b. Write an algorithm for computing the CDC (Controllability don't care) set for a logic network. (06 Marks)

Module-4

- 7 a. Illustrate resource sharing in Hierarchical sequencing graphs. (08 Marks)
 b. Discuss resource sharing and binding for non-scheduled sequencing graphs. (08 Marks)

OR

- 8 a. Write ASAP and ALAP scheduling algorithms. Find mobility of operations for a sequencing graph for the set of computations given in Q2 (a). (12 Marks)
 b. Write Hu's algorithm for resource constrained scheduling. (04 Marks)

Module-5

- 9 a. Minimize the incompletely specified state diagram given in Fig. Q9 (a) and also draw the minimum state diagram. (06 Marks)

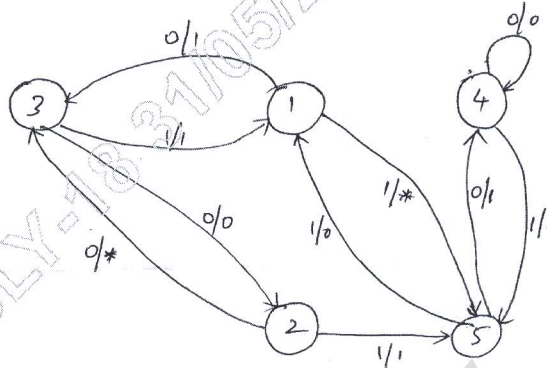


Fig. Q9 (a)

- b. Write FEAS algorithm to minimize cycle time and hence retime the network given in Fig. Q9 (b) to minimize cycle time. (10 Marks)

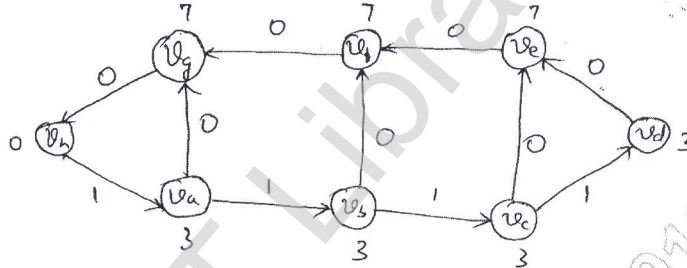


Fig. Q9 (b)

OR

- 10 a. Discuss testability considerations for synchronous circuits. (10 Marks)
 b. Extract state transition diagram from the given synchronous network shown in Fig. Q10 (b). (06 Marks)

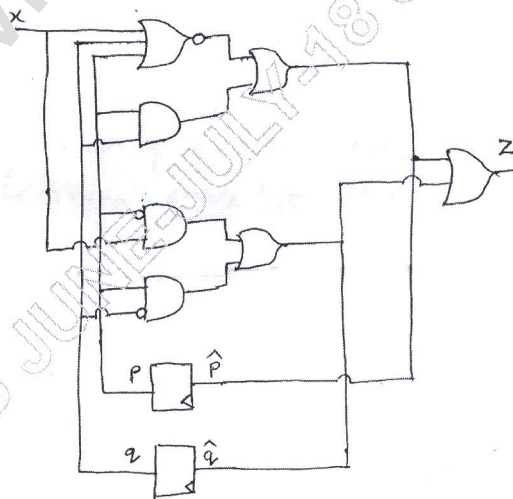


Fig. Q10 (b)
