CBCS Scheme

USN | | | | | | | | | | |

17/16EVE22

Second Semester M.Tech. Degree Examination, June/July 2018
VLSI Testing

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing one full question from each module.***

Module-1

1 a. What is a fault? Discuss fault models in use today with examples. **(10 Marks)**

b. What is breaks? With a circuit diagram, explain types of breaks. **(06 Marks)**

OR

2 a. What is logic simulation? Explain simulation process with the help of neat diagram. **(06 Marks)**

b. List the types of simulation? Explain compiled simulation with the help of synchronous and asynchronous circuit models. **(10 Marks)**

Module-2

3 a. Find the Boolean difference with respect to x_2 given in logic circuit shown in Fig.Q3 (a) below. **(06 Marks)**

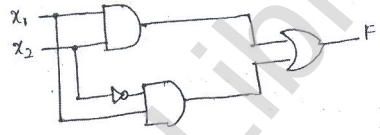

Fig. Q3 (a)

b. Explain PODEM algorithm function with neat diagram. **(10 Marks)**

OR

4 a. Explain Reed-Muller expansion technique for direct implementation. **(08 Marks)**

b. Explain extraction of a single cube and a double cube. **(08 Marks)**

Module-3

5 a. Explain Redundancy and its classifications with a testable circuit. **(08 Marks)**

b. Explain testable PLA design using Khakbaz's approach. **(08 Marks)**

OR

6 a. Explain homing tree sequence for Machine – N with state table and example. **(06 Marks)**

b. Explain test generation based on functional fault models using state table with examples and also list the steps involved in state encoding process. **(10 Marks)**

Module-4

7 a. Explain controllability and observability with a neat block diagrams. **(08 Marks)**

b. Explain how the AdHOC design rules are used for improving testability with examples. **(08 Marks)**

OR

8 a. Explain the scan path technique for testable sequential circuit design with examples. **(08 Marks)**

b. Explain LSSD design rules and advantages of the LSSD technique. **(08 Marks)**

Module-5

9 a. List the classification of test pattern generation approaches for BIST scheme and explain any one with example. **(08 Marks)**

b. Explain BILBO architecture with the help of neat block diagram. **(08 Marks)**

OR

10 a. Explain RAM fault model, with neat block diagram. **(08 Marks)**

b. Explain BIST technique for RAM chip using SRAM architecture. **(08 Marks)**

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