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14EVE41

Fourth Semester M.Tech. Degree Examination, June/July 2018

Synthesis and Optimization of Digital Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain custom and semi custom design styles/methodologies. **(10 Marks)**

b. What is synthesis? Explain different levels of synthesis. **(10 Marks)**

2 a. With respect to graphs, define following:
i) walk ii) forest iii) loop iv) trail **(04 Marks)**

b. For function $f = ab + ab'd + bcd'$, calculate:
i) Boolean difference with respect to variable 'a' and variable 'b'.
ii) Consensus with respect to variable 'c' and variable 'd'.
iii) Smoothing with respect to variable 'a' and variable 'd'.
iv) Uniteness with respect to 'a' and 'b' **(08 Marks)**

c. Write branch and bound algorithm and explain. **(08 Marks)**

3 a. Write structural and behavioral representation of full adder in VHDL. **(10 Marks)**

b. With example define following optimization techniques:
i) Tree height reduction
ii) Constant and variable propagation
iii) Operator strength reduction
iv) Loop expansion
v) Dead code elimination **(10 Marks)**

4 a. For PLA write tabular and symbolic representation of the function $f_1 = a'b' + b'c + ab$, $f_2 = b'c$. **(06 Marks)**

b. Write positional cube representation of the two input three output function $f_1 = a'b' + ab$, $f_2 = ab$, $f_3 = ab' + a'b$. **(06 Marks)**

c. Write definitions for the following:
i) Multiple output implicant
ii) Minimum cover
iii) Irredundant
iv) Prime **(08 Marks)**

5 a. In multilevel logic network, define below terms:
i) Decomposition
ii) Extraction
iii) Simplification
iv) Substitution **(08 Marks)**

b. Assuming functions are expressed in algebraic model, find $f_{quotient}$ and $f_{reminder}$ for
i) $f_{dividend} = ac + ad + bc + db + e$
$f_{divisor} = c + d$
ii) $f_{dividend} = ka + kb + f$
$f_{divisor} = a + b$ **(06 Marks)**

c. Consider logic network shown in Fig.Q5(c). Assume that data ready times of the primary inputs are $t_a = 0$ and $t_b = 10$. Let the propagation delay of the internal vertices be $d_g = 3$, $d_h = 8$, $d_m = 1$, $d_k = 10$, $d_\ell = 3$, $d_n = 5$, $d_p = 2$, $d_x = 2$ and $d_y = 3$.

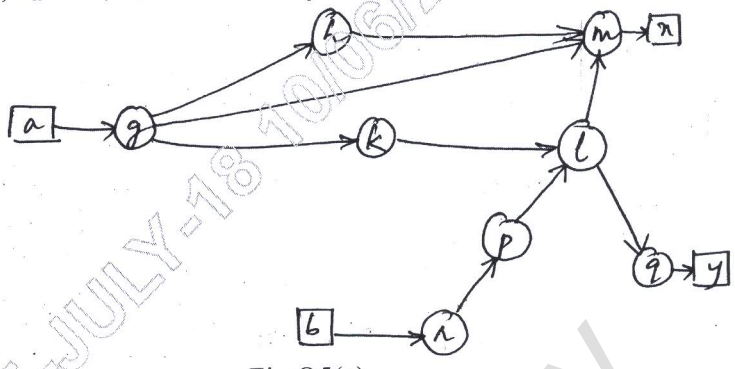

Fig.Q5(c)

Calculate maximum data ready time and topological critical path. **(06 Marks)**

6 a. Define non-hierarchical synchronous logic network. **(04 Marks)**

b. For a given synchronous logic network as shown Fig.Q6(b). Write set of equations.

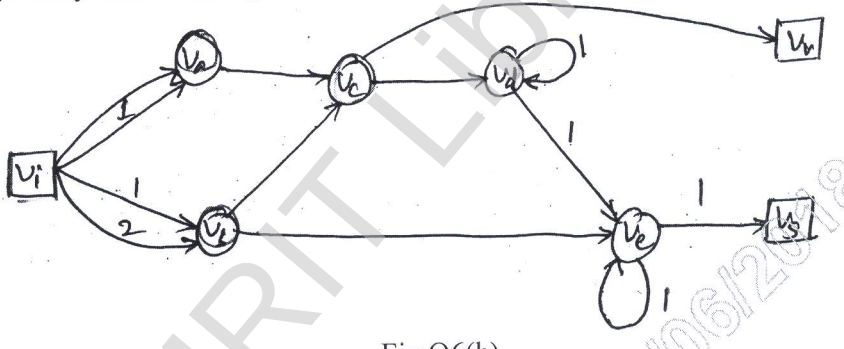

Fig.Q6(b) **(06 Marks)**

c. Write short note on following with respect to sequential circuit optimization:
   i) State encoding
   ii) State minimization **(10 Marks)**

7 a. Write and explain list scheduling algorithm. **(08 Marks)**

b. What are the conditions for minimum latency scheduling problem under resource constant in ILP form? **(06 Marks)**

c. Write about scheduling with pipelined resources. **(06 Marks)**

8 a. Write pattern tree for the following library cells with NAND as base function:
   i) AND2 ii) NOR2 iii) AOL21 **(06 Marks)**

b. What is network covering? Explain with an example. **(04 Marks)**

c. Write short note on any two:
   i) Antifuse FPGA
   ii) Design for testability
   iii) Automatic test pattern generator (ATPG) **(10 Marks)**

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