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14EVE421

Fourth Semester M.Tech. Degree Examination, June/July 2018

Advances in VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Compare CMOS and Bi-CMOS technology. **(05 Marks)**

b. Derive an expression for the pinch off voltage in a MESFET with an active layer thickness of t. **(10 Marks)**

c. Analyze the working of MOSFETs as switches. **(05 Marks)**

2 a. Calculate the threshold voltage for a realistic n-channel MIS device given the following: $N_a = 10^{17}$ cm^{-3}, $Q_i = 10^{11}$ g/cm^2, d = 20 nm and ϕ_{ms} = -0.95 V **(10 Marks)**

b. Analyze the working of a MODFET with neat diagrams. **(10 Marks)**

3 a. With the help of a neat diagram analyze the working of an ideal and non-ideal MIS structure. **(10 Marks)**

b. Bring out the effect of decrease in the physical separation between the source and the drain, with relevant equations, in a MOSFET. **(10 Marks)**

4 a. Determine the thickness of the Si active layer in a partially depleted SOI device if the layer is only 50% depleted in equilibrium. Assume that the Schottky barrier height is 0.72 eV, the effective density of states within the conduction band is $N_c = 3.22 \times 10^{19}$/cm^3, and the doping concentration is 10^{16}/cm^3. Assume that all of the donors are ionized. **(10 Marks)**

b. Analyze the working of carbon nano tubes with relevant diagrams. Also bring out the advantages and disadvantages of the same. **(10 Marks)**

5 a. Derive the equation for propagation time of a long polysilicon line. **(10 Marks)**

b. Design a NAND and NOR gate (Two input) using nMOS pass transistor. **(10 Marks)**

6 a. Analyze the concept of charge sharing. Give a methodology to overcome this problem. **(10 Marks)**

b. With relevant diagrams analyze the latch up problem in bulk CMOS technology. **(10 Marks)**

7 a. Analyze a clocking circuit working principle. Also bring out the mechanism of clock generation, clock distribution and clocked storage elements with relevant diagrams. **(10 Marks)**

b. Design a 3-input tally circuit with pass transistors. **(10 Marks)**

8 a. Using NOR-NOR logic implement Y = (A + B + C)(D + E + F). **(10 Marks)**

b. Analyze the working of RAM based FPGA with neat diagrams. **(10 Marks)**

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