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16/17EVE/ELD23

Second Semester M.Tech. Degree Examination, June/July 2018
Advances in VLSI Design

Time: 3 hrs.
Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1. a. Discuss different methodologies used in implementation of digital circuit. **(08 Marks)**
   b. With the help of neat diagrams, explain standard cell layout methodology. **(08 Marks)**

OR

2. a. Design a cell based programmable logic block by using multiplexers as function generators using truth table. **(08 Marks)**
   b. Explain programmable mesh-based interconnect network with figure. **(08 Marks)**

Module-2

3. a. Mention the different types of parasitic effects. Explain cross talk in dynamic circuits. **(08 Marks)**
   b. With the help of neat circuit diagrams, equations, explain how propagation delay of long wires are reduced. **(08 Marks)**

OR

4. a. Explain dynamic reduced swing networks using suitable diagrams. **(08 Marks)**
   b. Explain current and voltage mode transmission techniques using circuit diagrams. **(08 Marks)**

Module-3

5. a. With the help of a neat block diagrams, explain plesiochronous interconnect. **(06 Marks)**
   b. Define clock skew. Explain positive and negative clock skew. **(10 Marks)**

OR

6. a. Explain H-tree clock distribution network. **(08 Marks)**
   b. With the help of neat circuits, explain self timed pipelined datapath. **(08 Marks)**

Module-4

7. a. Explain the architecture for N-word memory with suitable diagrams. **(08 Marks)**
   b. With the help of a neat circuit diagram, explain the working of 4 × 4 OR ROM cell array. **(08 Marks)**

OR

8 a. Determine the values of the data stored at addresses 0, 1, 2, 3 in the ROM shown in Fig.Q8(a) and explain.
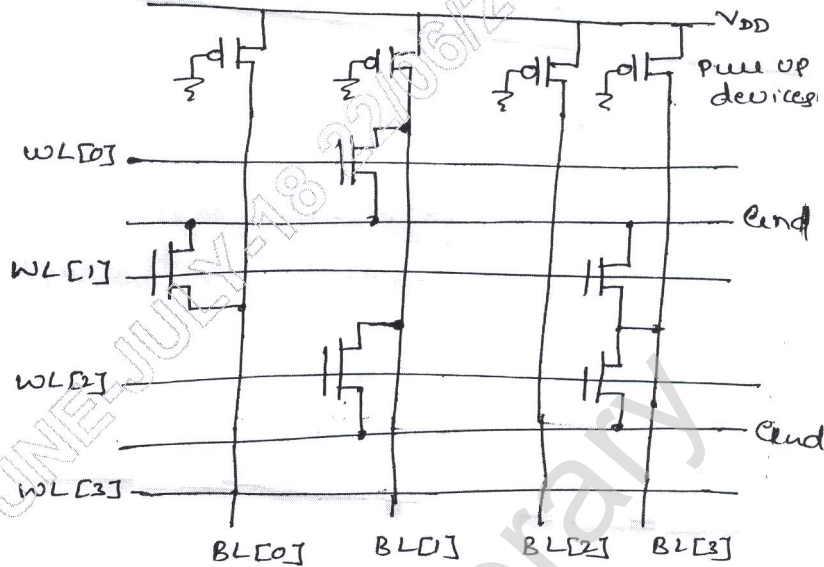

Fig.Q8(a) (08 Marks)

b. Explain all the three basic operations in a NOR flash memory with suitable figures.
(08 Marks)

Module-5

9 a. Explain open bit line and folded bit line architecture. (08 Marks)
   b. Explain redundancy and error correction in memory. (08 Marks)

OR

10 a. Discuss sources of power dissipation in memories. (08 Marks)
   b. Explain data retention in SRAMS. (08 Marks)

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