Fourth Semester M. Tech. Degree Examination, Dec. 2018/Jan. 2019

Advances in VLSI Design

Time: 3 hrs Note: Answer any FIVE full questions. Max. Marks: 100

- What are MOS devices? Explain saturation, linear and cut-off regions using drain current equations for MOS devices.
 - Explain with suitable circuit diagram the implementations of a simple BICMOS inverter. Also explain the two main issues with this simple BICMOS inverter implementation.

(08 Marks)

- With a neat sketch describe the structure of a MODFET and explain the band diagrams 2 associated with this structure.
 - b. Consider an n-channel MOSFET with the following information $N_a = 5 \times 10^{16}$ cm⁻³, $\mu_a^1 = 500 \text{ cm}^2/\text{V-S}, \ \varphi = 5 \times 10^{10} \text{ a/cm}^2, \ z = 50 \ \mu\text{m}, \ d = 30 \ \text{nm}, \ L = 5 \ \mu\text{m}, \ n_i = 10^{10} \ \text{cm}^{-3},$ $K_o = 3.9$, $E_g = 1.12$ eV, K = 11.9.
 - i) Determine the drain current at a gate voltage $V_G = 2V$ and drain voltage $V_D = 1V$.
 - ii) Consider the case when the gate voltage is 3V and drain voltage is 4V.
- Calculate the cut-off frequency of n-channel MOSFET with channel length = 1 μ , with 3 ρ -type substrate $\mu_n^1 = 1200 \text{ cm}^2/\text{VS}$, threshold voltage $V_T = 1.1 \text{ V}$ and $V_G = 5 \text{V}$ and z = 10.
 - With the help of neat sketches and mathematical expressions, explain the short channel (06 Marks) effects in MOSFET.
 - Explain MIS system in equilibrium.

(10 Marks)

- Show that in constant electric field scaling the threshold voltage and drain current scale 4 linearly with dimensions and voltage.
 - What are super buffers? Explain operations of NMOS super buffer circuit with neat figure (08 Marks) and stick diagram.
- For a NMOS PTL based 2 input NAND gate, give the modified truth table, the resulting 5 (12 Marks) K-MAP and one implementation of the function.
 - b. Explain carbon nanotubes.

(08 Marks)

- With a neat diagram, explain the difference between LUMO states and Homo states in 6 a. molecular diode under forward and reverse basis conditions. (09 Marks)
 - Realize NAND implementations of NMOS 4:1 MUX using depletion mode transistor and a dynamic CMOS 4:1 MUX using a clocked precharge pull-up. (11 Marks)
- With a suitable example, explain the following: 7
 - i) Hierarchy
- ii) Regularity
- iii) Modularity
- iv) Locality

(12 Marks)

- b. Realize 4-bit tree network using tally circuit and draw its stick diagram.
- (08 Marks)

- Explain the following: 8
 - Programmable structure Standard cell design
- b. Barrel shifter
- d. Full custom design

(20 Marks)

