

CBCS SCHEME

USN

--	--	--	--	--	--	--	--	--	--

16/17EVE/ELD23

Second Semester M.Tech. Degree Examination, Dec.2018/Jan.2019 Advances in VLSI Design

Time: 3 hrs

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. With the help of neat diagrams, explain standard cell layout methodology. (08 Marks)
b. Explain semicustom design flow. (08 Marks)

OR

- 2 a. With the help of a neat diagram, explain pre-diffused arrays. (08 Marks)
b. Explain array based programmable logics with suitable circuits. (08 Marks)

Module-2

- 3 a. Explain briefly capacitance and reliability cross talk using suitable equivalent circuits. (06 Marks)
b. Explain different approaches to reduce RC delay. (10 Marks)

OR

- 4 a. With the help of a neat diagrams and suitable equations, explain reduced swing circuit. (08 Marks)
b. Explain current mode transmission techniques. (08 Marks)

Module-3

- 5 a. With the help of a suitable diagram, explain asynchronous interconnect. (05 Marks)
b. Explain synchronous timing using suitable diagrams. (05 Marks)
c. Explain briefly clock jitter using suitable equations and waveforms/clocks. (06 Marks)

OR

- 6 a. Explain latch based clocking using suitable diagrams. (09 Marks)
b. With the help of a neat circuit diagram, explain the concept of arbiters. (07 Marks)

Module-4

- 7 a. Explain how do you classify memory based on different parameters. (07 Marks)
b. Explain three transistor dynamic memory cell. (09 Marks)

OR

- 8 a. With the help of a neat circuit diagram, explain basic differential sense amplifier circuit. (07 Marks)
b. Explain voltage down converters using suitable circuit diagrams. (09 Marks)

Module-5

- 9 a. Explain noise sources in IT-DRAM. (08 Marks)
b. Write short notes on memory yield. (08 Marks)

OR

- 10 a. With the help of a neat block diagram, explain sources of power dissipation in memories. (10 Marks)
b. Explain pseudo NMOS Programmable Logic Array (PLA). (06 Marks)

* * * * *