IISN		14ELD41
USIN		

Fourth Semester M. Tech. Degree Examination, Dec. 2017/Jan. 2018 **Advanced Computer Architecture**

Time:	3 hrs.	
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Max. Marks:100

	Note: Answer	any l	FIVE full	questions.
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1 a.	Briefly	explain the seven	dimensions	of MIPS	and	80×86	ISAs.
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(10 Marks)

Explain about Quantitative principles of computer design.

(06 Marks)

Explain the trends in cost of computer.

(04 Marks)

Explain dynamic branch prediction and branch prediction buffers. 2 a.

(08 Marks)

Explain in detail: data dependences and Hazards with examples.

(08 Marks)

Explain the technique to eliminate the stall for the hazards in DSUB AND and OR instruction with diagrams.

(04 Marks)

Explain Tomasulo's algorithm. Explain the differences in fields and registers used in tis 3 a. (10 Marks) application with and without speculation.

Explain Branch target buffers and their operation with diagrams. b.

(06 Marks)

c. Discuss the pros and cons of

Fallacy: processors with lower CPIS will be faster

Fallacy: processors with faster clocks will always faster.

(04 Marks)

What are the expectations of ideal processor for ILP? Explain the expectations. Discuss the (10 Marks) realizable processors for ILP.

Discuss the optimizations for cache performance to make the whole system faster. (10 Marks)

Discuss the RAID systems and the recovery processes with diagram, 5

(10 Marks)

Explain Poisson's distribution for a random variable from errors and failures.

(10 Marks)

Explain Global code scheduling in detail with a code fragment as example. 6

(10 Marks)

Explain Hardware support to preserve exception behavior.

(10 Marks)

A directory based cache coherence protocol requires overcoming. The problems related to 7 snooping protocol without use of Broadcast. Discuss. (10 Marks)

Discuss the advantages of different communication mechanisms.

(10 Marks)

Discuss the following:

- Virtual processing in opetron
- b. Translation look aside buffer
- Return address predictors
- Loop unrolling exploit ILP.

(20 Marks)