Fourth Semester M.Tech. Degree Examination, Dec.2017/Jan.2018 Synthesis & Optimization of Digital Circuits

Time: 3 hrs.

(Max. Marks:100

Note: Answer any FIVE full questions.

- 1 a. Write the difference between custom design and semicustom design. (04 Marks)
 - b. Briefly explain circuit views and levels of abstraction with the help of Y-chart. (06 Marks)
 - c. Write branch and bound algorithm. With the help of an example explain the algorithm.

(10 Marks)

- 2 a. Write the condition for a perfect graph. with the help of an example explain perfect graph.

 (04 Marks)
 - b. What is ITE operator? Write the ROBDD for the function ac + bc using ITE operator.
 (06 Marks)
 - c. Find the longest path in the graph shown in Fig. Q2 (c) using Bellman-Ford algorithm.
 (10 Marks)

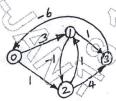


Fig. Q2 (c)

- a. Write the VHDL code for a finite state machine that recognizes two or more consecutive one's in an input data stream. (06 Marks)
 - b. Explain various types of data flow based transformations.

(14 Marks)

- 4 a. Consider the function f = ab + ac + a. Write the cover of the function and check whether the function is tautology or not (10 Marks)
 - b. Consider the function f = abc + abc + abc + abc. With abc as don't care condition. Write the ON set, OFF set and DC set of the function. Apply the Expand operator and find the minimum cover. (10 Marks)
- 5 a. Consider the logic network with primary input variables {a, b, c, d, e} and primary output variables {w, x, y, z} described by the following equations.

$$p = ce + de$$

$$q = a + b$$

$$r = p + a$$

$$s \Rightarrow r + \overline{b}$$

$$\sqrt{}=ac+ad+bc+bd+e$$

$$u = qc + qc + qc$$

$$v = ad + bd + cd + ae$$

$$\mathbf{w} - \mathbf{v}$$

$$\mathbf{x} = \mathbf{s}$$

$$y = t$$

$$z = u$$

Write the logic network for the equations. Apply the transformations like elimination, decomposition, extraction and simplification, substitution and write the final logic network.

(14 Marks)

5 b. Consider the network with the following equations:

 $f_x = ad + bd + cde + ge$

f = abc

Find the kernel and co-kernel of the function.

(06 Marks)

6 a. Briefly explain rule based systems for logic optimization.

b. Briefly explain about detection of false paths.

(08 Marks) (05 Marks)

c. For the FSM shown in Fig. Q6 (c), obtain the minimum state diagram.

(07 Marks)

0/1 30/0 1/0 1/1

Fig. Q6 (c)

7 a. Explain the Adhoc testing.

(10 Marks)

b. Explain the terms LUT FPGAs and antifuse based FPGAs.

(10 Marks)

- Write a note on any four of the following:
 - a. Automatic test pattern generator,
 - b. Test Access Port. (TAP)
 - c. BIST architecture.
 - d. Tree based covering.
 - e. ALAP scheduling algorithm.

(20 Marks)

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