Fourth Semester M.Tech. Degree Examination, Dec.2017/Jan.2018
Advances in VLSI Design

Time: 3 hrs.   Max. Marks:100

Note: *Answer any FIVE full questions.*

1 a. Describe with suitable mathematical analysis, the transfer plot of CMOS inverter and also explain the role of aspect ratios of n-channel and p-channel MOSFET's in CMOS device. **(10 Marks)**

   b. With the help of energy band diagrams, explain the working of MESFET under (i) Thermal equilibrium (ii) Forward bias   (iii) Reverse bias. **(10 Marks)**

2 a. Explain the basic principles of modulation doping with the help of energy band diagrams and hence explain the operations of HEMT device structure formed using GaAs and AlGaAs. **(08 Marks)**

   b. List the ideal properties of MIS systems. **(04 Marks)**

   c. A JFET has $N_a = 10^{19}\,cm^{-3}$, $N_d = 10^{16}\,cm^{-3}$, $a = 0.1\,\mu m$, $L = 10\,\mu m$ and $Z = 1\,mm$. Assume that the device is S_i with an intrinsic concentration of $10^{10}\,cm^{-3}$ and a relative dielectric constant of 11.8. Assume also that in saturation the square law can be used and that the value of I_{D_0} is 5 μA. Calculate (i) Built-in voltage   (ii) Pinch off voltage (iii) $V_{D_S Sat}$ if $V_G = -2V$ (iv)   Drain current if $V_D = 1V$ and $V_G = -2$ V.   Take $\frac{KT}{q} = 0.0259$, $n_i = 10^{10}\,cm^{-3}$, $q = 1.6\times10^{-19}$, $\in_0 = 8.85\times10^{-14}$ F/cm. **(08 Marks)**

3 a. Derive an expression for the threshold voltage of an MIS device and hence explain enhancement and depletion modes of operation. **(08 Marks)**

   b. Briefly discuss the sources of oxide charges and hence define flat band voltage. **(06 Marks)**

   c. Calcuulate the minimum capacitance for an n-channel (p-type) MIS capacitor. Assume that the capacitor is made from the Si-SiO-A*l* materials system. The p-type doping concentration within the semiconductor N_a is $5\times10^{16}\,cm^{-3}$, the oxide thickness d is 12 nm, the insulator relative dielectric constant is 3.9, intrinsic concentration is $10^{10}\,cm^{-3}$, semiconductor relative dielectric constant is 11.8, $\frac{KT}{q} = 0.0259$ V and $\in_o = 8.85\times10^{-14}$ F/cm, $n_i = 10^{10}\,cm^{-3}$. **(06 Marks)**

4 a. Show that in a short channel FET, the drain current is less than that in a long channel FET due to high electric field. **(06 Marks)**

   b. Briefly explain the processing challenges to further CMOS miniaturization. **(08 Marks)**

   c. Show that the threshold voltage and drain current scale linearly with dimensions and voltage in constant electric field scaling method. **(06 Marks)**

5 a. Describe the construction and working of SOI MOSFET. Also discuss its advantages over conventional MOSFET. **(08 Marks)**

   b. What is tactile computing? With examples, compare tactile computing with conventional computing. **(04 Marks)**

   c. Sketch the molecular diode energy levels under equilibrium, forward bias and reverse bias. Explain each in brief. **(08 Marks)**

6   a.   Explain the working of nMOS inverting super buffer with the help of a neat circuit diagram and stick diagram.   **(05 Marks)**
   b.   Realize 2-input NAND gate using BiCMOS gates.   **(04 Marks)**
   c.   With the help of truth table, K-map and nMOS realization, design pass transistor logic for,
   (i) 2-input NOR gate   (ii) 2-input EXOR gate.   **(05 Marks)**
   d.   Derive an expression for propagation delay in terms of capacitive load (C_L), gate capacitance (C_g) for a 2-input NOR gate driving a super buffers for different fanout values.   **(06 Marks)**

7   a.   Explain the conceptual layout of 3-input tally circuits. Draw the stick diagram for pass transistor based 3-input tally circuit.   **(08 Marks)**
   b.   With a neat diagram, explain the CMOS implementation of 4 : 1 multiplexer.   **(06 Marks)**
   c.   Explain with an example, line search algorithm.   **(06 Marks)**

8   a.   Explain the following terms with an example each:
   (i) Hierarchy   (ii) Regularity   (iii) Modularity   (iv) Locality.   **(10 Marks)**
   b.   What is programmable logic? Explain programmable logic structures with diagrams.   **(10 Marks)**

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