CBCS Scheme

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16/17EVE12

First Semester M.Tech. Degree Examination, Dec.2017/Jan.2018
Digital VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing one full question from each module.***

Module-1

1 a. Derive the MOSFET current equation in different regions of operation and plot the current voltage characteristics of an n-channel MOSFET. **(08 Marks)**

b. What is MOSFET scaling? Explain in brief the types of scaling indicating the effect of scaling on derive characteristics. **(08 Marks)**

OR

2 a. Explain the working of resistance load inverter with necessary circuit diagram and voltage transfer characteristic. Also device the equations for V_{OL}, V_{OH}, V_{IL} and V_{IH}. **(08 Marks)**

b. Calculate the critical voltage V_{OL}, V_{OH}, V_{IL} and V_{IH} and find the noise margins of the depletion load inverter circuit with the following parameter :

$V_{DD} = 5V$, $V_{TO(driver)} = 1.0V$, $V_{TO(load)} = -3.0V$, $\left(\frac{W}{L}\right)_{Driver} = 2$, $\left(\frac{W}{L}\right)_{Load} = \frac{1}{3}$,

$K_{n(driver)} = k_{n(load)} = 25\mu A/V^2$, $\gamma = 0.4\,V^{\frac{1}{2}}$, $\phi_F = -0.3V$. **(08 Marks)**

Module-2

3 a. Draw the circuit of a CMOS inverter and derive the switching threshold (V_{th}) equation for the same. **(06 Marks)**

b. Define propagation delay time and obtain the equations for τ_{PHL} and τ_{PLH} for CMOS inverter. **(10 Marks)**

OR

4 a. Derive an equation for switching power dissipation of CMOS inverter with necessary circuit diagram and waveforms. **(06 Marks)**

b. How to measure the propagation delay of an inverter using ring oscillator? Explain with necessary diagrams and equations. **(06 Marks)**

c. With suitable circuit diagrams and equations, explain RC delay model to calculate the interconnect delay. **(04 Marks)**

Module-3

5 a. With necessary circuit diagrams, explain the following dynamic RAM cells. 4T DRAM, 3T DRAM, 2T DRAM and IT DRAM. **(10 Marks)**

b. Explain 4bit ×4bit NAND based ROM array with necessary diagrams. **(06 Marks)**

OR

6 a. Briefly explain memory structure of SRAM with read and write circuitry with the help of read and write timing diagrams. **(10 Marks)**

b. Draw the schematic of flash memory cell and explain. **(06 Marks)**

Module-4

7 a. With necessary circuit diagram explain enhancement load based rationed, 3bit dynamic shift register. **(08 Marks)**

b. Discuss the working principle of NORA CMOS logic and zipper CMOS logic with necessary diagrams. **(08 Marks)**

OR

8 a. What is BiCOMS logic? With neat circuit diagram explain the working of BiCMOS inverter? Also mention the advantages and disadvantages of BiCMOS. **(10 Marks)**

b. Draw the BiCMOS circuit for the function $Y = \overline{A(B+C)}$. **(04 Marks)**

c. Calculate the value of V_{out} in the circuit shown in Fig. Q8(c), if threshold voltage of pass transistor is 0.7V. **(02 Marks)**

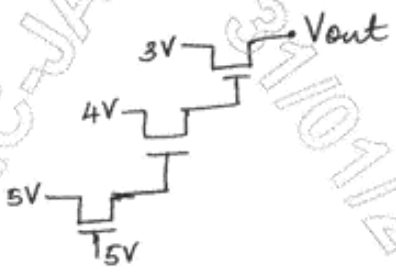

Fig. Q8 (c)

Module-5

9 a. With relevant circuit diagram and symbolic representation, explain two types of input circuits. **(08 Marks)**

b. Explain on-chip clock generation and clock distribution with necessary diagrams. **(08 Marks)**

OR

10 a. What is latch up in CMOS? Explain with necessary diagrams and equations? Also discuss guidelines for avoiding latch up. **(10 Marks)**

b. Describe performance modeling procedure with a model. **(06 Marks)**

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