CBCS Scheme

USN | | | | | | | | | |

16/17EVE14

First Semester M.Tech. Degree Examination, Dec.2017/Jan.2018
Low Power VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Explain the needs of low power VLSI design. **(05 Marks)**

b. Derive the expression for power dissipation in CMOS circuit due to charging and discharging of capacitance. **(07 Marks)**

c. Explain the basic principles of low power design. **(04 Marks)**

OR

2 a. Discuss the terms capacitive power dissipation, internal switching energy and static state power with respect to gate level logic simulation. **(08 Marks)**

b. Discuss Monte Carlo power simulation. **(08 Marks)**

Module-2

3 a. Define static probability. Derive the equation that relates the static probability P of memoryless random logic signal to its expected frequency 'f'. **(08 Marks)**

b. What is entropy? Discuss the power estimation of combinational logic using entropy. **(08 Marks)**

OR

4 a. Derive the relationship between the power dissipation and the stage ratio for an inverter chain. **(08 Marks)**

b. Write a note on low power digital cell library. **(08 Marks)**

Module-3

5 a. Explain local restructuring rules of transformation with relevant illustrations. **(08 Marks)**

b. With the help of an example, explain the precomputation logic optimization method to trade area for power in a synchronous digital circuit. **(08 Marks)**

OR

6 a. Explain the clock driving schemes for clock distribution. Also discuss the techniques used for delay reduction. **(08 Marks)**

b. What is tolerable skew? With neat waveforms, explain the terms double clocking and zero clocking. Write the expressions to avoid them. **(08 Marks)**

Module-4

7 a. Briefly explain the principle of guarded evaluation and bus multiplexing for switching activity reduction. **(08 Marks)**

b. Draw the control data flow graph for the equation $Y_n = a_n b_n + 3a_{n-1}$. Also write the corresponding hardware architecture to reduce area. **(08 Marks)**

OR

8 a. Discuss 16-bit carry skip adder with constant block width and variable block width. **(08 Marks)**

b. Explain 8-bit Wallace Tree multiplier. **(08 Marks)**

Module-5

9 a. Explain the sources of power dissipation in DRAM and SRAM. **(08 Marks)**

b. For low power CAD framework, explain the design flow with supporting tools. **(08 Marks)**

OR

10 a. Explain capacitance models for hardware modules and activity models for data and control signals, with respect to architectural estimation. **(08 Marks)**

b. Write a note on adiabatic computation. **(08 Marks)**

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