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Internal Assessment Test-II

Sub:	MICROPROCESSORS						Code:	15EC42	
Date:	16/04 / 2018	Duration:	90 mins	Max Marks:	50	Sem:	4th	Branch:	ECE(A,B, C,D)
Answer FIVE FULL Questions									

OBE

Marks CO RBT

1. Briefly explain the operations of the following string instructions of 8086, [3+3+2+ CO2 L2
indicating the initializations required to use them: 2]

(i) CMPSB, (ii) MOVSB, (iii) LODSB, (iv) STOSB.

CMPS; compare String Bytes ^{source to destination} on String word

It can be used to compare string byte or string word.

- Length of the string must be in CX register.*
- If both the byte or word strings are equal zero flag is set.*
- The DS:SI and ES:DI point to the two strings, The REP instruction prefix is used to repeat the operation till CX becomes zero, or the condition specified by REP prefix is false.*

```

MOV AX, SEG 1
MOV DS, AX
MOV AX, SEG 2
MOV ES, AX
MOV SI, offset string 1
MOV DI, offset string 2
MOV CX, 010H
CLD
REPE CMPSB ; compare 010H words of string 1
and string 2 while they are equal
If a mismatch found, update the flag register execution.

```

MOVSB/movsw: (move string byte or string word)

The MOVSB/movsw instruction ~~also~~ moves a string of bytes/words pointed to by DS:SI register pair (source) to the memory location pointed to by ES:DI pair (destination).

The REP instruction prefix is used with MOVSB instruction to repeat it by a value given in the CX.

- After MOVSB instruction is executed once, the index registers are updated and CX decremented automatically.

LODS: Load string byte or string word

The LODS instruction loads the AL/AX reg. by the content of a string pointed to by DS:SI register pair.

SI is modified automatically depending on DA.

If byte transfer (LODSB): SI modified by 1.
(LODSW): SI " " 2.

No other flags are affected.

STOS: store string byte or word:-

The STOS instruction stores the AL/AX register contents to a location in the string pointed by ES:DI register pair.

DI is modified accordingly. No flags are affected by this instruction.

2. What are assembler directives? Explain any five assembler directives with [10] CO2 L2 example.

An assembler is a program used to convert an assembly language program into the equivalent machine code modules which may further be converted to executable codes.

- It decides the address of each label and substitutes the values for each of the constants and variables.

DB (Define Byte) :- Used to reserve a byte or bytes of memory locations available in memory.

- While preparing .exe file this directive directs the assembler to allocate the specified no. of memory bytes to the said data type that may be a constant, variable, string etc.

```
NI DB 01H, 02H, 03H, 04H
```

→ Reserve four memory locations and initialize them with the specified values.

```
MSH DB 'Good Morning'
```

- Reserve the no. of bytes of memory equal to no. of characters.

DW (define word); Reserves words or words of memory locations in the available memory.

```
NI DW 1234H, 4567H, 7890H, 045CH
```

- Reserves 4 words in memory, initialize the words with specified values.

Assume; Assume logical segment Name

- It is used to inform the assembler the names of the logical segments to be assumed for different segments used in the program.

Assume CS: CODE ⇒ directs assembler that the machine codes are available in a segment named CODE.

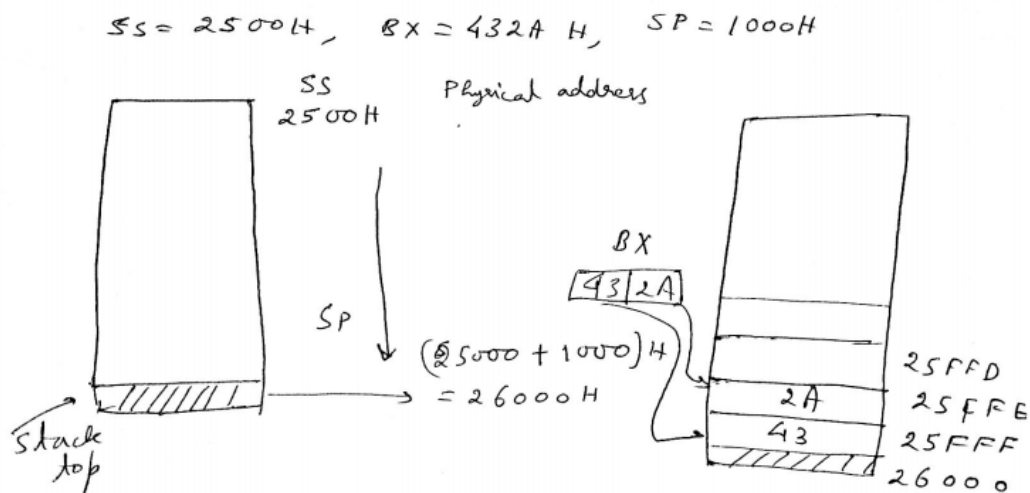
END: END of Program: It marks the end of an assembly language program.

Assembler ignores the source lines available after END directive.

ENDP: End of procedure.

In ALP, subroutines are called procedures. The procedures may be independent program modules, which return particular results or values to the calling programs.

- 3.(a) Sketch the content of stack memory indicating the value of SP register before PUSH BX operation and after the PUSH BX operation. Assume SS = 2500 H, BX = 432AH and SP = 1000 H. [04] CO4 L3



- (b) Write a program to generate 100 ms delay using 8086 microprocessor operating at 10 MHz frequency. Show calculation for delay. [06] CO3 L3

Solution: The time delay program is as follows:

	Instruction	T-states for each instruction
	MOV BX, Count	4
L1:	DEC BX	2
	NOP	3
	JNZ L1	16
	RET	8

In this program, the instructions DEC BX, NOP, and JNZ L1 form the loop as they are executed repeatedly until BX becomes zero. Once BX becomes zero, the 8086 returns to the main program.

- Number of clock cycles for execution of the loop once (n) = 2 + 3 + 16 = 21
- Time required for the execution of loop once = $n \times T = 21 \times 1/(10 \times 10^6) = 2.1 \mu s$
- Count = $td/(n \times T) = 100 \times 10^{-3} / (2.1 \times 10^{-6}) = 47619$ (BA03).
- By loading BA03H in BX, the time taken to execute the delay program is approximately 100ms.
- The NOP included in the delay program is to increase the execution time

of the loop. To get more delay, the number of NOP instructions in the delay loop can be increased.

The exact delay obtained using this time delay subroutine can be calculated as shown below,

The MOV BX, Count & RET instructions in the delay program are executed only once. The JNZ instruction takes 16 T-states when the condition is satisfied (i.e. ZF= 0) and 4 T – states when the condition is not satisfied, which occurs only once.

Exact delay = [4 x 0.1 + (2+3) x 47619x 0.1 + 16 x 47618 x0.1 + 4 X 0.1 + 8 x 0.1] μs

$$=99.9999\text{ms}$$

$$=100\text{ms.}$$

4.(a)	<p>What are the methods that can be used to pass parameters to a procedure? Explain anyone of them with an example.</p> <p><u>Passing parameters to procedures</u></p> <ul style="list-style-type: none"> (i) Using global declared variable (ii) Using registers of CPU architecture (iii) Using memory locations (reserved) (iv) Using stack (v) Using PUBLIC and EXTRN <p>(i) <u>Using global declared variables</u></p> <pre> assume CS: code1, DS: Data Data segment Number equ 77h global Data ends code1 segment start: mov ax, data mov mov DS, ax : mov AX, number : code ends assume CS: code 2 code 2 segment mov AX, DATA mov DS, AX mov BX, NUMBER code 2 ends end start </pre>	[06]	CO3	L3		
(b)	<p>Differentiate between procedure and macro.</p> <table border="0" style="width: 100%;"> <tr> <td style="vertical-align: top; width: 50%;"> <p><u>Macro</u></p> <ul style="list-style-type: none"> i) complete code of the instructions string is inserted at each place where the macro-name appears. ii) Hence lengthy EXE file iii) Does not use stack; </td> <td style="vertical-align: top; width: 50%; border-left: 1px solid black;"> <p><u>Subroutine</u></p> <ul style="list-style-type: none"> i) control of execution is transferred to the SR, every time it is called. ii) smaller EXE file. iii) Utilizes stack service. </td> </tr> </table>	<p><u>Macro</u></p> <ul style="list-style-type: none"> i) complete code of the instructions string is inserted at each place where the macro-name appears. ii) Hence lengthy EXE file iii) Does not use stack; 	<p><u>Subroutine</u></p> <ul style="list-style-type: none"> i) control of execution is transferred to the SR, every time it is called. ii) smaller EXE file. iii) Utilizes stack service. 	[04]	CO3	L2
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5.	<p>What are the sequence of actions taken by 8086 and the device, when a device interrupts 8086 over INTR line? Explain about the software and reserved internal interrupts of 8086.</p>	[10]	CO4	L3		

Interrupt - To break the sequence of operations. While the CPU is executing a program, an 'interrupt' breaks the normal sequence of execution of instructions, diverts its execution to some other program called Interrupt Service Routine (ISR).

While one interrupt is being served, another interrupt may appear.

- ISR are the programs to be executed by interrupting the main program execution of the CPU, after an interrupt request appears.

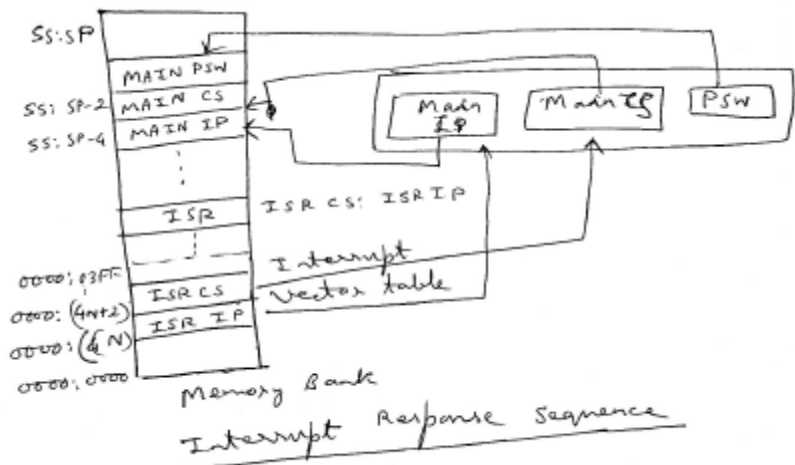
After the execution of ISR, the main program continues the execution further from the point at which it was interrupted.

- Say, an external device interrupts via $\sim V$ at the interrupt pin (NMI or INTR) while CPU is executing an instruction of a program.

- CPU completes the execution of the current instruction

- IP is incremented to the point to the next instruction.

- If it is NMI, TRAP or divide by zero CPU acknowledges immediately on its \overline{INTA} pin.
- If it is INT request, CPU checks IF.
- If $IF = 1$, \overline{INTA} goes low (acknowledged)
- If $IF = 0$, interrupt requests are ignored.
- CPU computes the vector address from the type of the interrupt, that may be passed to the interrupt structure of the CPU internally (in case of S/W interrupts, NMI, TRAP and divide by zero) or externally.
- IP and CS point to the next instruction to be executed after ISR, CS, IP and PSW pushed to stack.
- ~~IF~~ - IF is cleared.
- TF is cleared after every response to the single step interrupt.
- The new address of ISR found from the interrupt vector table.
- ISR executes.
- During ISR execution if some other interrupt to be service served, $IF = 1$ once more by ISR of the 1st interrupt.
- If IF is not ~~set~~ the subsequent interrupts won't be acknowledged, till the current one is ~~is~~ completed.
- At the end of ISR, the last instruction should be IRET.
- When IRET is executed, the contents of flags, IP and CS are retrieved to the respective registers.
- Execution continues.



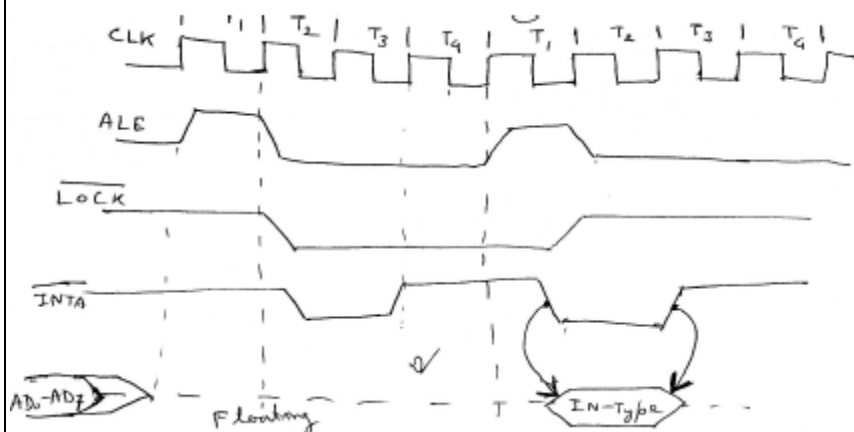
Type 0	ISR IP ISR CS	0000:0000 0000:0002	Reserved for divide by zero interrupt
Type 1	ISR IP ISR CS	0000:0004 0000:0006	
Type 2	ISR IP ISR CS	0000:0008 0000:000A	Reserved for NMI
Type 3	ISR IP ISR CS	0000:000C 0000:000E	Reserved for INT single byte instruction
Type 4	ISR IP ISR CS	0000:0010 0000:0012	Reserved for INTO instruction.
	ISR IP ISR CS	0000:0014 0000:0016	
Type N	ISR IP ISR CS	0000:004N 0000:(004N+2)	Reserved for two byte instruction INT type.
Type FFH	ISR IP ISR CS	0000:03FE 0000:03FF	

- For the INTR signal, to be responded to in the next instruction cycle, it must go high in the last clock cycle of the current instruction or before that
- If INTR request appears after the last clock cycle of the current instruction, it will be responded to after the execution of the next instruction,

IF=1 → processor responds to INTR interrupt.
 IF=0, → " does not respond to INTR.

Once processor responds to INTR, IF=0

- External signal interrupts the processor.
- ALE pulse appears after interrupt signal, preventing use of bus for any other purpose.
- \overline{LOCK} goes low at the trailing edge of the first ALE pulse.
- \overline{LOCK} remains low till the next machine cycle
- At trailing edge of \overline{LOCK} , \overline{INTA} goes low and remains ~~low~~ low for two clock states before returning back to the high state.
- It remains high till the start of the next machine cycle. (till next trailing edge of ALE)
- Then \overline{INTA} again goes low, remains low for two states, before returning to the high state.
- The first trailing edge of ALE floats the ~~bus~~ bus AD_0-AD_7 , while the second trailing edge prepares the bus to accept the type of the interrupt.
- The type of interrupt remains on the bus for a period of two cycles.



6.(a) Write an ALP to convert Hexadecimal number to BCD number.
 .MODEL SMALL
 .DATA
 HEXN DW 0FFFFH
 TEN DW 000AH

[06] CO4 L3

	<pre> BCD DB 3 DUP (00H) .CODE MOV AX, @DATA MOV DS, AX MOV CL, 04H MOV AX, HEXN AGAIN: XOR DX, DX DIV TEN MOV BCD[DI], DL XOR DX, DX DIV TEN ROL DL, CL OR BCD[DI], DL INC DI CMP AX, 00H JNE AGAIN MOV AH, 4CH INT 21H END </pre>			
(b)	<pre> Create a macro that would find the logical NAND value of two operands. .MODEL SMALL .DATA NUM1 DW 4556H NUM2 DW 0FFFFH RES DW 0000H .CODE LOGNAND MACRO N1, N2 MOV AX,N1 MOV BX,N AND AX, BX NOT AX ENDM MOV AX, @DATA MOV DS, AX2 LOGNAND NUM1, NUM2 MOV RES, AX MOV AH, 4CH INT 21H END </pre>	[04]	CO3	L3

7.	<p>Write an alp which replaces all occurrences of character '-' in a given string by '*'. .MODEL SMALL .DATA SOURCE DB 'C-M-R', '\$' COUNT EQU 5H SEARCH DB '-' .CODE MOV AX, @DATA MOV DS, AX MOV ES, AX LEA DI, SOURCE MOV AL, SEARCH MOV CX, COUNT CLD BACK: SCASB JNZ NEXT DEC DI MOV BYTE PTR [DI], '*' INC DI NEXT: LOOP BACK LEA DX, SOURCE MOV AH, 09H INT 21H MOV AH, 4CH INT 21H END</p>	[10]	CO2	L3
8.(a)	<p>Write an ALP to find whether the given number is 2 out of 5 code. .MODEL SMALL .DATA NUM DB 09H MSG1 DB 'NUMBER IS 2 OUT OF 5 CODE', '\$' MSG2 DB 'NUMBER IS NOT A 2 OUT OF 5 CODE', '\$' .CODE MOV AX, @DATA MOV DS, AX MOV AL, NUM MOV CX, 03H FIRST: ROL AL, 01H JC LAST LOOP FIRST MOV CX, 05H SECOND: ROL AL, 01H ADC BL, 00H LOOP SECOND CMP BL, 02H JNE LAST LEA DX, MSG1</p>	[06]	CO2	L3

	<pre> JMP SKIP LAST: LEA DX, MSG2 SKIP: MOV AH, 09H INT 21H MOV AH, 4CH INT 21H END </pre>			
(b)	<p>Write an ALP which computes the factorial of an 8-bit number. The factorial value to be maximum 8-bit in size.</p> <pre> .MODEL SMALL .STACK 64H .DATA NUM1 DB 05H FACTRES DB 00H .CODE MOV AX, @DATA MOV DS, AX MOV AL, NUM1 CALL FACTN MOV FACTRES, AL MOV AH, 4CH INT 21H FACTN PROC NEAR MOV BL, AL MOV AL, 01H CMP BL, 00H JE L1 AGAIN: MUL BL DEC BL JNZ AGAIN L1: RET FACTN ENDP END </pre>	[04]	CO2	L3