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Internal Assesment Test-III

Sub:	MICROPROCESSORS							Code:	15EC42
Date:	21/05/ 2018	Duration:	90 mins	Max Marks:	50	Sem:	4th	Branch:	ECE(A,B)

Answer FIVE FULL Questions

		Marks	OBE	
			CO	RBT
1.	Draw and discuss the typical minimum mode of operation of 8086.	[10]	CO1	L2

Minimum mode of 8086 system and timings

For minimum mode MN/$\overline{MX}$ = 1

- Only one microprocessor in minimum mode system.
- Other components are latches, transreceivers, clock generator, memory and I/O devices.
- chip selection logic required.

Latches are buffered O/P D-type flip flops, eg. 74LS373 or 8282.

- Used for separating valid address from the multiplexed address/data signals.
- Controlled by ALE signal.

Transreceivers : Bidirectional buffers.
controlled by $\overline{DEN}$ and DT/$\overline{R}$.

$\overline{DEN}$ = 0, valid data available on the data bus.
DT/$\overline{R}$ = 0, to the processor (receiving)
DT/$\overline{R}$ = 1, from the processor (transmitting)

Working of minimum mode configuration system

- Read cycle begins in T_1 with the assertion of ALE and M/$\overline{IO}$ signal.
- During HIGH of ALE, valid address is latched on the local bus.
- At T_2, address is removed from local bus and sent to the O/P.
- Bus is then tristated.
- $\overline{RD}$ signal activated in T_2
- $\overline{RD}$ goes low — valid data available on data bus.

- $\overline{RD}$ causes the addressed device to enable its data bus drivers.
- Addressed device will drive the READY line high.
- As read signal goes to high level, data bus is tristated.

$M/\overline{IO} = 0$, indicate I/O operation

$M/\overline{IO} = 1$ " - Memory operation

- Write cycle begins with the assertion of ALE and emission of the address.
- In T_2, after sending the address in T_1, the processor sends the data to be written to the addressed location.
- Data remains on bus, until the middle of T_4 state.
- $\overline{WR}$ becomes active at the beginning of T_2

$M/\overline{IO}$	$\overline{RD}$	$\overline{DEN}$	Transfer type
0	0	1	I/O Read
0	1	0	I/O write
1	0	1	Memory read
1	1	0	Memory write

CS_o → chip select odd

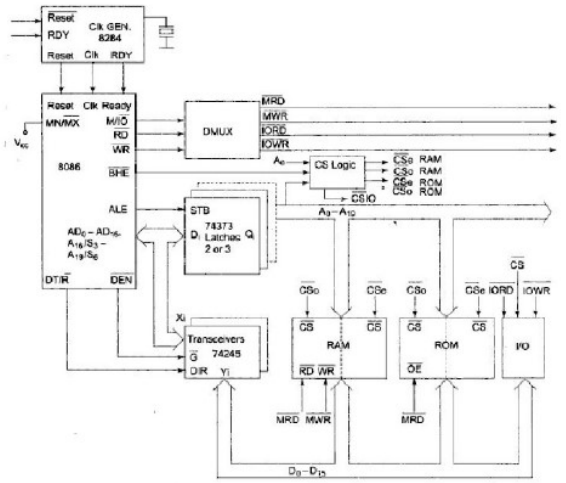
CS_e → chip select even

HOLD response sequence

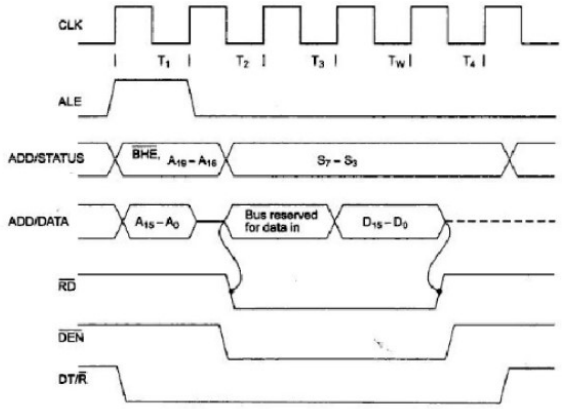
HOLD pin is checked at the end of each cycle.

- If it is active before T_4 of the previous cycle or during T_1 of the current cycle, CPU activates HLDA in the next clock cycle and for the succeeding bus cycles, bus will be given to another requesting master.
- Bus control is not regained by the processor, until the requesting master drops the HOLD pin low.

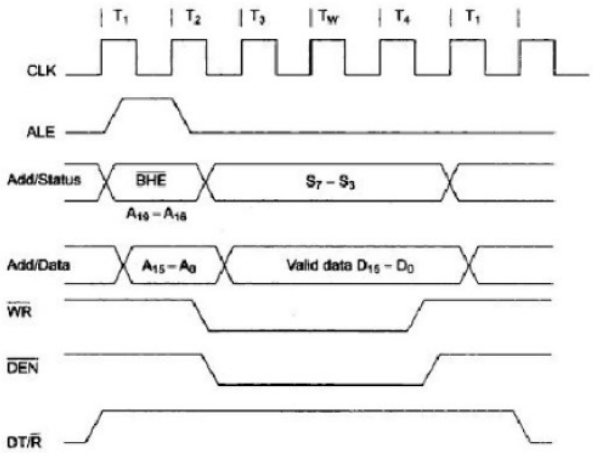
Minimum mode of 8086



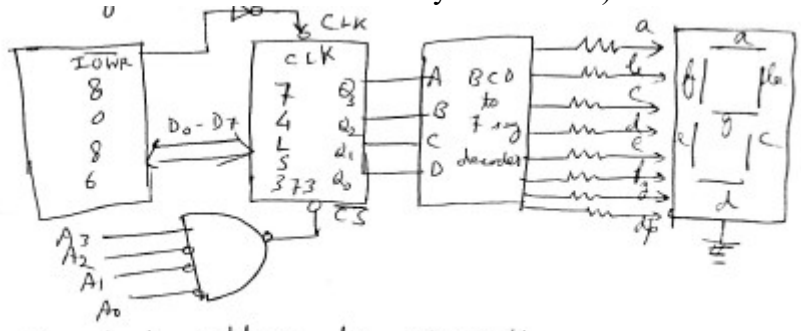
Read Cycle Diagram for Minimum Mode



Write Cycle Diagram for Minimum Mode

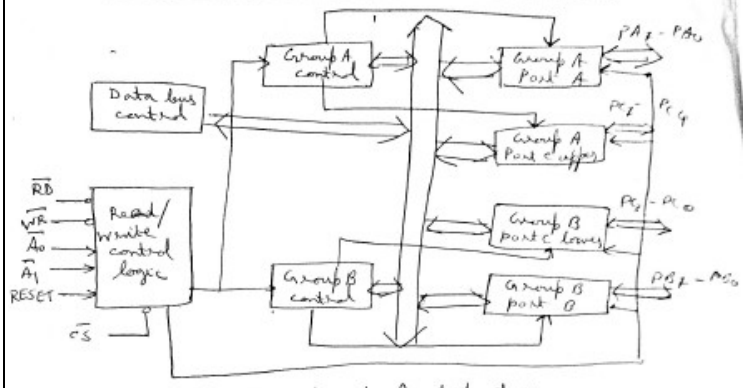


2.	Interface a 7-segment LED using a 74LS373 latch for I/O address 0Ch. Write a	[10]	CO5	L3

	program that simulates a single digit seconds counter (0-9) on the LED digit. (Assume a one second software delay is available).  Let port address be 08000H XX: MOV AL, 00H ~~XOR AL, AL~~ YY: OUT 08H, AL ; display 0H Call delay INC AL CMP AL, 0AH JZ XX JMP YY			
3.	Describe the architecture of 8255. Also explain I/O mode and BSR mode of operation of 8255.	[4+6]	CO5	L2

Architecture of 8255

PIO 8255 [programmable I/P - O/P port]



8255 Internal Architecture

$PA_7 - PA_0$ — either latched O/P or buffered I/P lines depending on the control word in control word register

$PC_7 - PC_4$ — upper nibble of port C lines. either O/P latches or I/P buffer lines. ~~control~~ handshaking for mode 1 or 2

$PC_3 - PC_0$ → lower PC lines. same as $PC_7 - PC_4$

$PB_0 - PB_7$ → latched O/P or buffered I/P

$\overline{RD}$ → low to indicate read operation to 8255

$\overline{WR}$ → low to indicate write

$\overline{CS}$ → If $\overline{CS} = 0$, 8255 responds to $\overline{RD}$ and $\overline{WR}$ signals

$A_1 - A_0$ → address I/P lines and are driven by MP

$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A_1	A_0	
0	1	0	0	0	Port A to data bus
0	1	0	0	1	Port B to data bus
0	1	0	1	0	Port C to data bus
0	1	0	1	1	CWR to data bus
1	0	0	0	0	Data bus to PA
1	0	0	0	1	Data bus to PB
1	0	0	1	0	Data bus to PC
1	0	0	1	1	Data bus to CWR
X	X	1	X	X	Data bus tristated
1	1	0	X	X	Data bus tristated

$D_0 - D_7$: Data bus lines those carry data or control word to/from the MP

RESET : Reset = High, clears control word Register

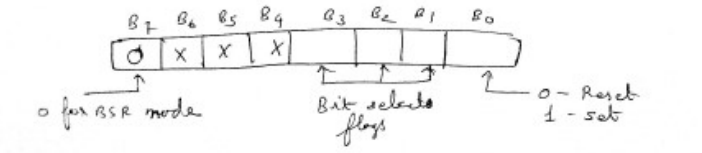
Modes of operation of 8255

I/O mode and BSR mode

BSR mode

Any of the 8-bits of PC can be set or reset depending on B_0 of the control word.

- The bit to be set or reset is selected by bit select flags B_3, B_2 and B_1 of the CWR



B_3	B_2	B_1	Selected Bit of Port C
0	0	0	B_0
0	0	1	B_1
0	1	0	B_2
0	1	1	B_3
1	0	0	B_4
1	0	1	B_5
1	1	0	B_6
1	1	1	B_7

I/O modes :—

MODE 0 (Basic I/O mode) :—

— Simple I/P and O/P capability using each of the three ports.

Features :—

i) Two 8-bit ports (port A and port B) and two 4-bit ports (port C upper and lower) —Two 4-bit ports can be combinedly used as third 8-bit port,

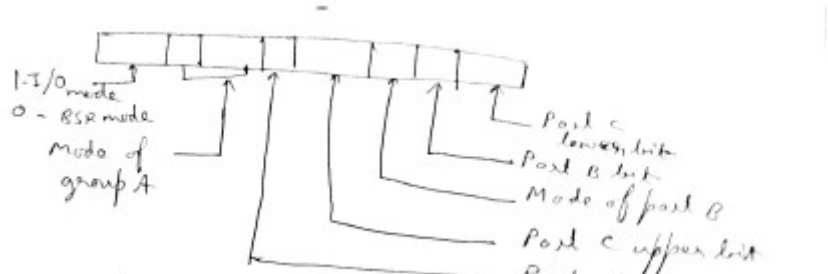
ii) Any port can be used as I/P or O/P port.

iii) O/P ports are latched, I/P ports are not latched

iv) A maximum of four ports are available.

∴ 16 I/O configurations are possible.

— Mode selection is done using a register interface to 8255, control word register.



Port B mode is either 0 or 1 depending on B_2 bit

ii) If port bit = 0, → port is O/P else port is I/P

Group A modes

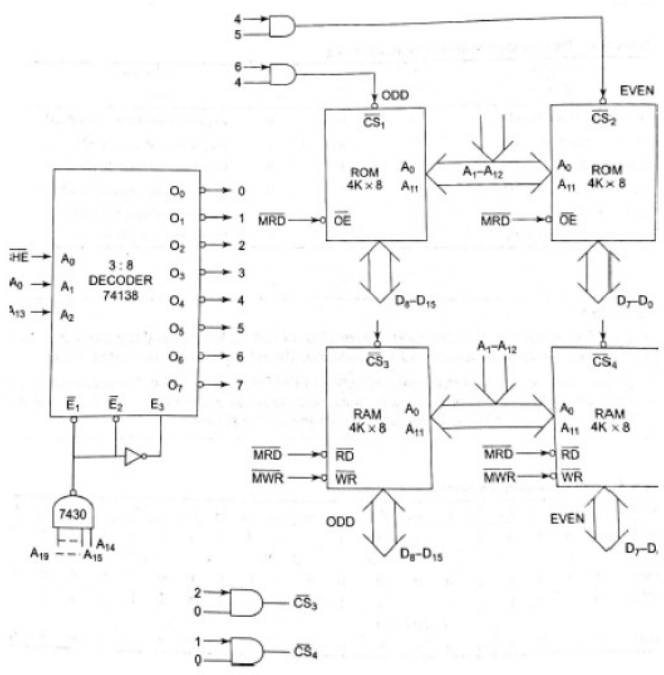
B_6	B_5	Mode
0	0	mode 0
0	1	mode 1
1	0	mode 2
1	1	X

I/O mode control register format

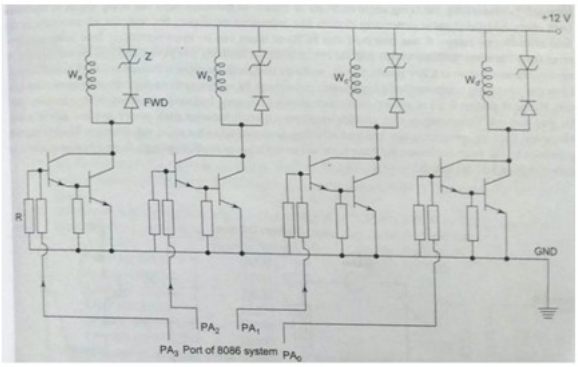
4.	Interface two 4K x 8 EPROM and two 4K x 8 static RAM chips to 8086. The addresses of RAM and ROM should start from FC000H and FE000H respectively.	[10]	CO5	L3

Table Memory Map for Problem

Address	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_{09}	A_{08}	A_{07}	A_{06}	A_{05}	A_{04}	A_{03}	A_{02}	A_{01}	A_{00}
FFFFFH	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
EPROM								8K×8												
FE000H	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
FDFFFH	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
RAM								8K×8												
FC000H	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0



5.	Interface a stepper motor to 8086 using 8255 and write a program to rotate the motor in clockwise direction 5 times. The 8255 port A address is 0740h. The stepper motor has 200 rotor teeth. The port A bit PA0 drives winding Wa, PA1 drives winding Wb and so on. The stepper motor has an internal delay of 10msec. Assume that the routine for this delay is already available. The stepper motor connections for all the four windings are shown in Fig. The ALP for rotating the shaft is,	[06]	CO5	L3




```
.CODE
        MOV AL,80H
        MOV DX,CWR
        OUT CWR,AL
        MOV CX,1000
        MOV AL,88H
        MOV DX,PORTA
AGAIN1:     OUT  DX, AL
        CALL DELAY
        ROR AL,01H
        DEC CX
        JNZ AGAIN1
        MOV AL,88H
MOV AX,4C01H
INT 21H
END
```

6. Describe the significance of different bits of control word register of 8254. Explain mode-2 operation of 8254 timer briefly. What is the control word to be used to operate counter-l in mode-2 binary? [5+2+3] CO5 L2

Control Register

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Control Word Format

SC_1	SC_0	OPERATION
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

SC-Select Counter Bit Definitions

RL_1	RL_0	OPERATION
0	0	Latch Counter for 'ON THE FLY' reading
0	1	Read/Load Least Significant Byte only
1	0	Read/Load MSB only
1	1	Read/Load LSB first then MSB

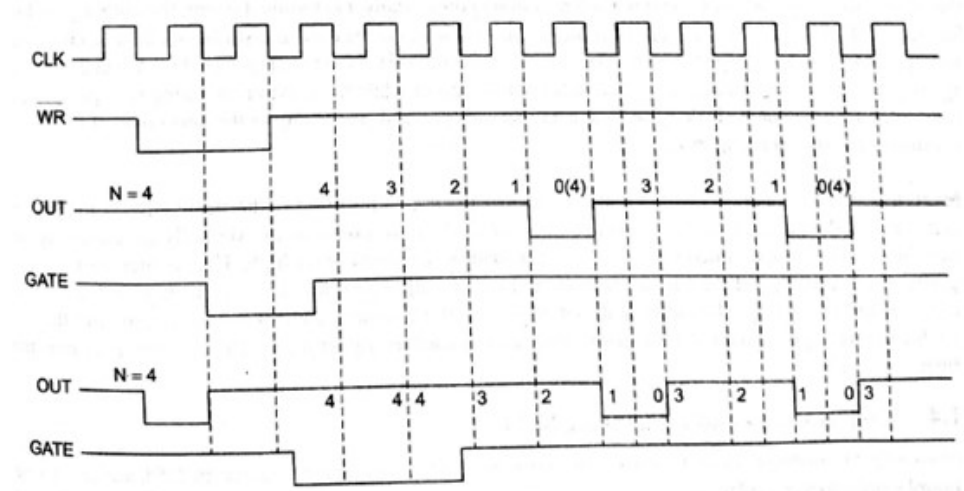
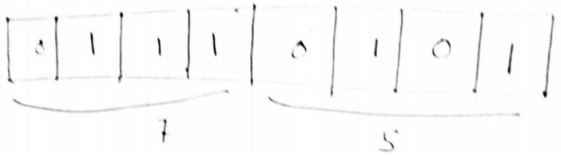
RL-Read/Load Bit Definitions

M_2	M_1	M_0	Selected Mode
0	0	0	Mode 0
0	0	1	Mode 1
x	1	0	Mode 2
x	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

$M_2M_1M_0$ Mode Select Bit Definitions

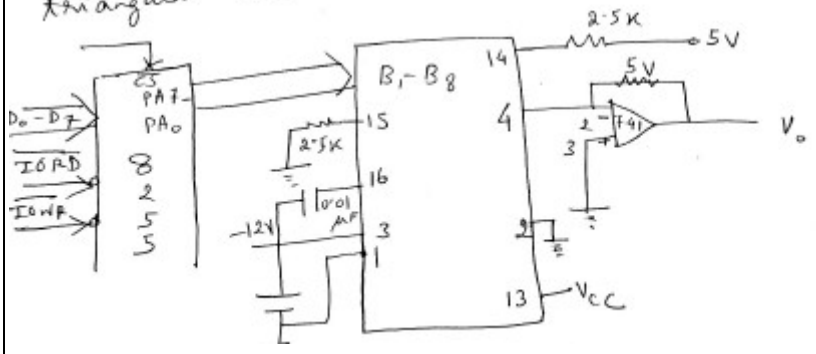
BCD	Operation
0	Hexadecimal Count
1	BCD Count

HEX/BCD Bit Definition

	Mode 2 (Rate generator or divide by N counter) Rate generator or divide by N counter If N is loaded as count value, after (N-1) cycles, the O/P becomes low for one clock cycle   counter-1 in mode-2 binary			
7.(a)	Describe the following keyboard handling INT 21h DOS functions: (i) Function 01h, (ii) Function 08h **INT 21H function 01**: Inputting a single character with echo – This function waits until a character is input from the keyboard echoes it to the monitor. After the interrupt, the input character AL. **INT 21H function 08H**: Inputting a single character without echo This function waits until a character is input from the keyboard, and the character is not displayed (or echoed) on the screen. After the interrupt, the input character will be in AL. MOV AH,08H ; keyboard input without echo INT 21H	[04]	CO6	L2
(b)	Write a program to generate triangular wave using DAC -0800.	[06]	CO5	L3

DAC 0800

Write an ALP to generate a triangular wave of frequency 500 Hz using the interfacing dkt. given. 8086 operates at 8 MHz. The amplitude of the triangular wave should be +5V



The required freq. of o/p = 500Hz.

$\therefore T = 2ms$.

Assume CS: code

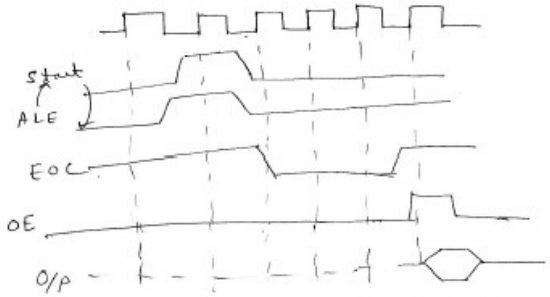
code segment

start:

```
        MOV   AL,80H
        MOV   DX,CWR
        OUT   DX, AL   ; Initialize 8255 ports
        MOV   AL,00
        MOV   DX, PA
B1:     OUT   DX, AL
        INC   AL
        CMP   AL, 0FFH
        JNZ   B1
B2:     OUT   DX, PA
        DEC   AL
        CMP   AL, 00
        JNZ   B2
        JMP B1
code ends
end start.
```

8.	Interface ADC 0808/0809 to 8086 using 8255 and write a program to convert the analog voltage connected to the second channel.	[10]	CO5	L3

Interface ADC 0808 with 8086 using 8255 ports. Use port A of 8255 for transferring digital data O/P of ADC to the CPU and Port C for control signals. Assume that an analog I/P is present at I/P_2 of the ADC and a clock I/P of suitable frequency is available for ADC. Draw the schematic and write required ALP.



give a high to low pulse at ALE.

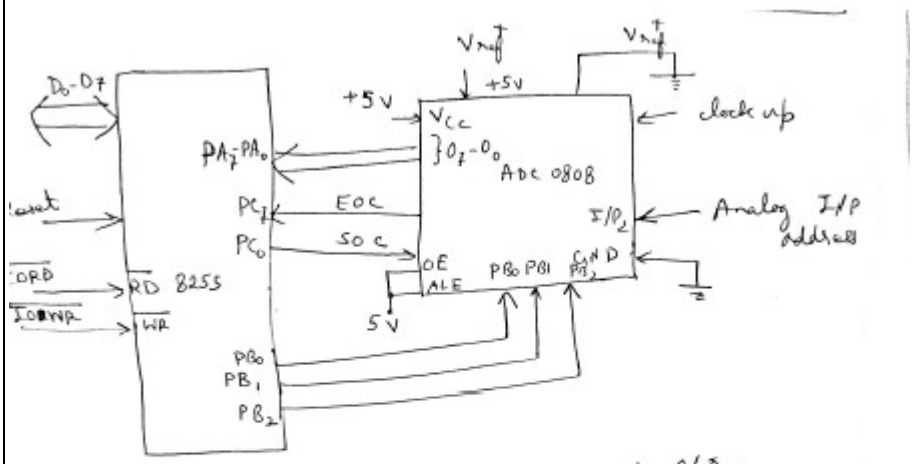
Make OE = 0

check for EOC for going high.

As EOC goes high give high to OE.

Read digital data

[when checking for EOC, maintain OE = 0]



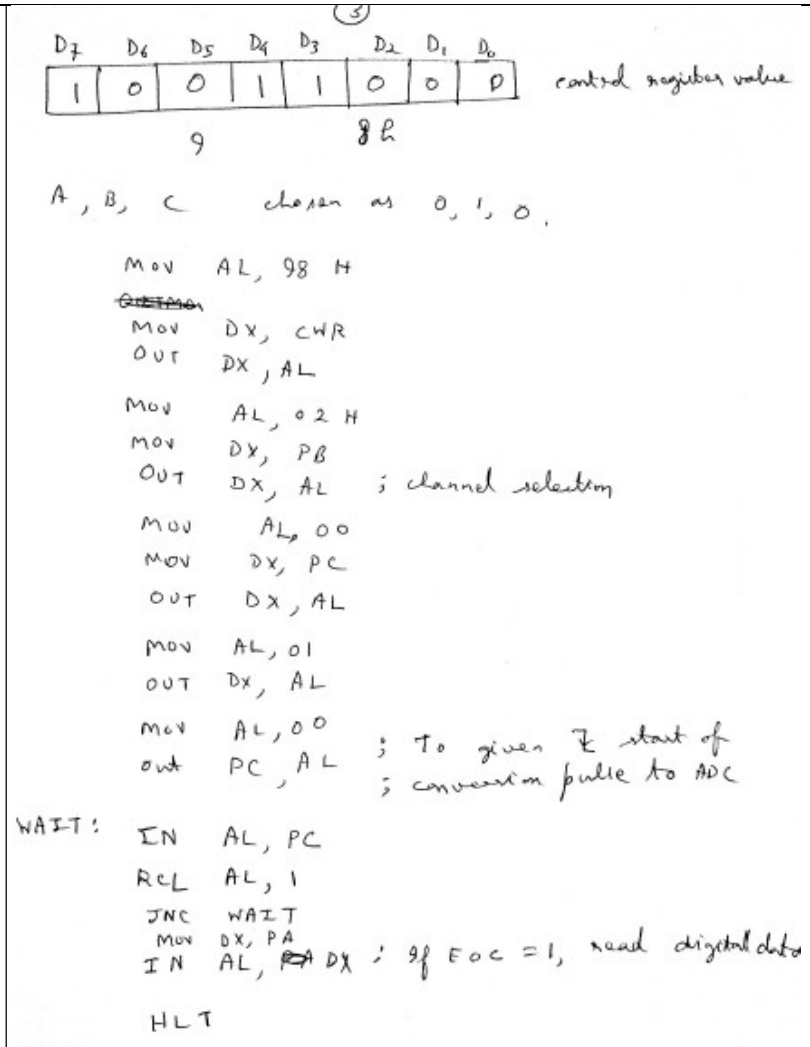
OE and ALE = high to enable the O/Ps.

PC upper as I/P.

PC lower " O/P.

PA 8 bit I/P port to read digital data

PB O/P to select the analog I/P channel.



9.(a)	Write a program in 8086 using DOS 21H interrupts which waits for a key to be pressed from the keyboard. If the key is 'G', display the message 'GOOD' on the CRT and display the message 'VERY GOOD' if the key 'V' is pressed. Display 'NOT VALID' if any other key is pressed.	[06]	CO6	L3

```
.MODEL SMALL
        .DATA
MSG1    DB   'ENTER THE CHARACTER',13,10,'$'
MSG2    DB   13,10,'GOOD',13,10,'$'
MSG3    DB   13,10,'VERY GOOD',13,10,'$'
MSG4    DB   13,10,'NOT VALID',13,10,'$'
        .CODE
        MOV AX,@DATA
        MOV DS, AX

        LEA DX, MSG1
        MOV AH, 09H
        INT 21H

        MOV AH, 01H
        INT 21H

        CMP AL, 'G'
```

```
                JNE NEXT1
                LEA DX, MSG2
                JMP LAST
NEXT1:          CMP AL,'V'
                JNE NEXT2
                LEA DX, MSG3
                JMP LAST
NEXT2:          LEA DX, MSG4
LAST:           MOV AH, 09H
                INT 21H
                MOV AH, 4CH
                INT 21H
                END
```

(b) Draw the timing diagram for $\overline{RQ}$ / $\overline{GT}$ for maximum mode. [04] CO1 L2

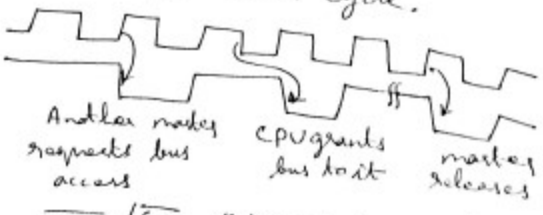
Timing for $\overline{RQ}$ / $\overline{GT}$ signals (Request / Grant signal)

- It consists of a sequence of three pulses.
- The request / grant pins are checked at each rising pulse of clock I/P.
- Request / Grant pins are used by other local bus masters in maximum mode
- Each of the pins is bidirectional with $\overline{RQ}$/$\overline{GT_0}$ having higher priority than $\overline{RQ}$ / $\overline{GT_1}$,

(i) A pulse one clock wide from another bus master requests the bus access to 8086

(ii) During T_4 (current) or T_1 (next) clock cycle, a pulse one clock wide from 8086 to the requesting master, indicates that 8086 has allowed the local bus to float and that it will enter 'hold acknowledge' state in the next clock cycle

(iii) A one clock wide pulse from another master indicate to 8086 that 'hold' request is about to end and 8086 may regain control of the local bus at the next clock cycle.



$\overline{RQ}$ / $\overline{GT}$ Timings in maximum mode