Q1. Derive an expression for drain current of a MOSFET in triode and saturation region.

Ans 1:

DERIVATION OF $I_D - V_{DS}$ RELATIONSHIP :-

G
W
t_{ox}
Oxide
Capacitor of value $C_{ox} W dx$
dx
Velocity dx/dt
Drain
Source channel
charge dq
$E = -\frac{dV(x)}{dx}$
$V(x)$
Voltage
V_{DS}
$dV(x)$
L
x

Let $V_{GS} > V_t$ is applied b/w G & S to induce channel also let V_{DS} is applied b/w D & S.

Considering operation in triode region for which channel is continuous & ∴ V_{GD} must be greater than V_t or $V_{DS} < V_{GS} - V_t$ where channel will have tapered shape shown in diagram.

For MOSFET, G & channel forms a ∥ plate capacitor with oxide layer as dielectric.

If C_{ox} = capacitance / unit area.

& t_{ox} = oxide layer thickness

∴ $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ — (2), where ϵ_{ox} = permittivity of SiO_2

$= 3.9\epsilon_0 = 3.9 \times 8.854 \times 10^{-12}$

$= 3.45 \times 10^{-11} F/m$

for $t_{ox} = 10nm$,

$C_{ox} = 3.45 \times 10^{-3} F/m^2$ or $3.45 fF/\mu m^2$.

Considering the infinitesimal strip of the gate at distance x from the S. Capacitance of this strip is $C_{ox} W dx$. To find the charge stored on this infinitesimal strip of the gate capacitance, the capacitance is multiplied by the effective V b/w G & channel at point x. Effective V is the V that is responsible for inducing the channel at point x & is thus $(V_{GS} - V(x) - V_t)$, where $V(x)$ is the voltage in the channel at point x. The $\bar{e}$ charge dq in the infinitesimal portion of the channel at point x i.e.

$$dq = -C_{ox}(W dx)[V_{GS} - V(x) - V_t] \quad (3) \qquad C = \frac{dq}{dv}.$$

-ve sign indicates dq is -ve charge. The V_{DS} produces an EF along the channel in the -ve x direction. At point x this field can be expressed as

$$E(x) = -\frac{dV(x)}{dx} \quad \text{—④}$$

EF $E(x)$ causes the $\bar{e}$ charge dq to drift toward the drain with a velocity dx/dt

$$\therefore \frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{dV(x)}{dx} \quad \text{—⑤}$$

where μ_n = $\bar{e}$ mobility in the channel (called surface mobility, whose value depends on fabrication process technology.

The resulting drift I (i) can be obtained as

$$i = \frac{dq}{dt} = \frac{dq}{dx} \times \frac{dx}{dt}$$

substituting for charge/unit length (dq/dx) from equa③ & for $\bar{e}$ drift velocity (dx/dt) from equa ⑤

$$i = -C_{ox}W\left[V_{GS} - V(x) - V_t\right] \times \mu_n \frac{dV(x)}{dx}$$

$$\Rightarrow i = -\mu_n C_{ox} W\left[V_{GS} - V(x) - V_t\right]\frac{dV(x)}{dx}$$

{ $\therefore$ Although evaluated at a particular point x, i is constant at all points along the channel. }

$\therefore i = i_D$ in magnitude

$$i_D = -i = \mu_n C_{ox} W\left[V_{GS} - V(x) - V_t\right]\frac{dV(x)}{dx} \quad \text{—⑥}$$

Integrating equa ⑥ on both sides from $x=0$ to $x=L$ & $V(0)=0$ to $V(L)=V_{DS}$.

$$\int_0^L i_D \, dx = \int_0^{V_{DS}} \mu_n C_{ox} W\left[V_{GS} - V(x) - V_t\right] dV(x)$$

$$\Rightarrow i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[\left[V_{GS} - V_t\right]V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad \text{—⑦}$$

equa. (7) is the expression for triode region of the $i_D - V_{DS}$ characteristics.

Equa. of I at the beginning of saturation region is found by substituting $V_{DS} = V_{GS} - V_t$.

$$\therefore i_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_t)^2 \quad \text{--- (8)}$$

equa (8) is the expression for $i_D - V_{DS}$ characteristic in saturation region; it gives the saturation value of i_D corresponding to the given V_{GS}. Saturation current i_D remains constant for a given V_{GS} as V_{DS} is varied.

$\mu_n C_{ox}$ = constant determined by the process technology. = known as process transconductance parameter $\Rightarrow k_n'$ (A/V^2)

$$\therefore k_n' = \mu_n C_{ox} \quad \text{--- (9)}$$

$$\therefore \text{For Triode region } i_D = k_n' \left(\frac{W}{L}\right) \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$\text{\& For saturation region } i_D = \frac{k_n'}{2} \left(\frac{W}{L}\right) (V_{GS} - V_t)^2$$

Q2a. Derive an expression for drain to source current i_{DS} and finite output resistance r_o in saturation, if channel length modulation is considered.

Ans 2a.

→ But practically when $V_{DS} > V_{DSsat}$, channel will be effected. As V_{DS} is increased, the channel pinch-off point is moved slightly away from the D towards S. Voltage across the channel remains constant at $V_{GS} - V_t = V_{DSsat}$ & the additional V applied to the D appears as a V drop across the narrow depletion region b/w the end of the channel & D region. This V accelerates the e's that reach the D end of the channel & sweeps them across the depletion region into D. When depletion region widens, the channel length is in effect reduced, from L to L−ΔL, a phenomenon called as CHANNEL-LENGTH MODULATION.

Source | channel | Drain

$- \; V_{DSsat} = V_{GS} - V_t \; +$ | $- \; +$ $V_{DS} - V_{DSsat}$

$L - \Delta L$ | ΔL

L

Now since i_D is inversely ∝ to channel length & $i_D \propto V_{DS}$ from equn. (14), $i_D = \frac{k_n'}{2} \frac{W}{L} V_{DS}^2$ in saturation region, i_D increases as V_{DS} increases. To account for the dependence of i_D on V_{DS} in saturation, L is replaced by L−ΔL in equn. (13)

$$i_D = \frac{k_n'}{2}\left(\frac{W}{L-\Delta L}\right)(V_{GS}-V_t)^2$$

$$\Rightarrow i_D = \frac{k_n'}{2}\left(\frac{W}{L}\right)\frac{1}{\left(1-\frac{\Delta L}{L}\right)}(V_{GS}-V_t)^2$$

∴ multiply both Numerator & Denominator by $L+\Delta L$

$$\Rightarrow i_D = \frac{k_n'}{2}\left(\frac{W}{L}\right)\left(1+\frac{\Delta L}{L}\right)(V_{GS}-V_t)^2 \quad \text{— (1)}$$

assuming $(\Delta L/L) \ll 1$ & assuming $\Delta L \propto V_{DS}$.

$$\Rightarrow \boxed{\Delta L = \lambda' V_{DS}}$$

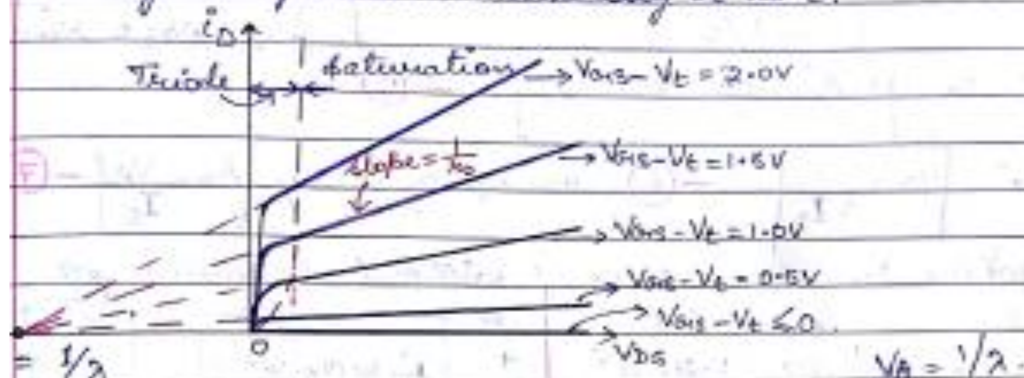
where λ' = process technology parameter = dimension (µm/V)

$$\therefore i_D = \frac{k_n'}{2}\left(\frac{W}{L}\right)\left(1+\frac{\lambda'}{L}V_{DS}\right)(V_{GS}-V_t)^2 \quad \text{— (2)}$$

$$\boxed{\lambda'/L = \lambda} \quad \therefore i_D = \frac{k_n'}{2}\left(\frac{W}{L}\right)(1+\lambda V_{DS})(V_{GS}-V_t)^2 \quad \text{— (3)}$$

where $\lambda = \frac{\lambda'}{L}$ = process technology parameter (V^{-1})

For a given process λ inversely $\propto$ to L.



Effect of V_{DS} on i_D in the saturation region, MOSFET parameter V_A depends on the process technology & for a given process is $\propto$ to channel length L.

equa. ③ shows the linear dependence of i_D on V_{DS} in saturation region. When the straight-line $i_D - V_{DS}$ characteristics are extrapolated they intercept the V_{DS} axis at the point $V_{DS} = -V_A$, where V_A = +ve. Voltage. Equa. ③ indicates that $i_D = 0$ at $V_{DS} = -1/\lambda$. ∴ $V_A = -V_{DS} = \frac{1}{\lambda}$

∴ V_A = process technology parameter with dimension (V)

For a given process $V_A \propto$ channel length (L).

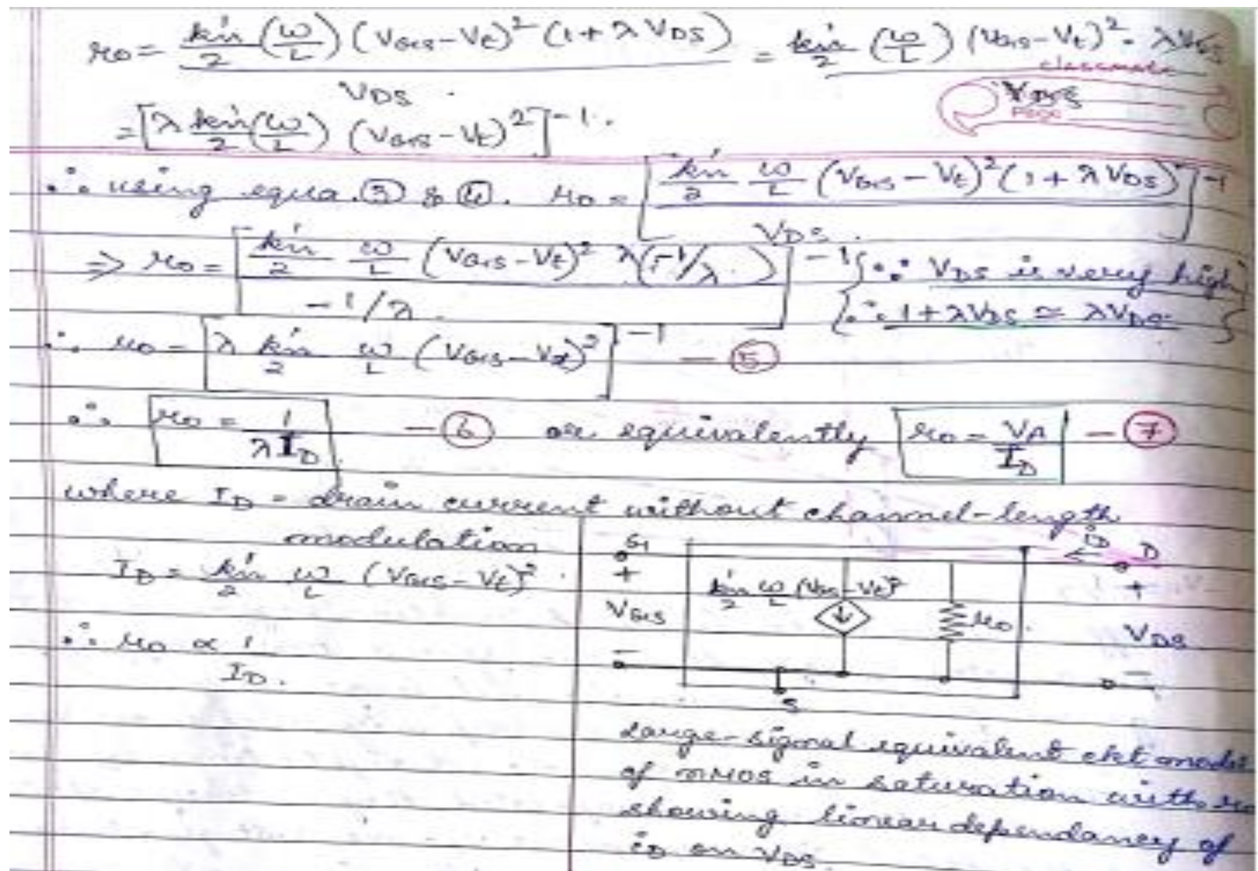
∴ $V_A \propto L$ $\Rightarrow V_A = V_A' L$.

where V_A' = process technology parameter with dimension (V/μm) = typical value = (6 − 50) V/μm

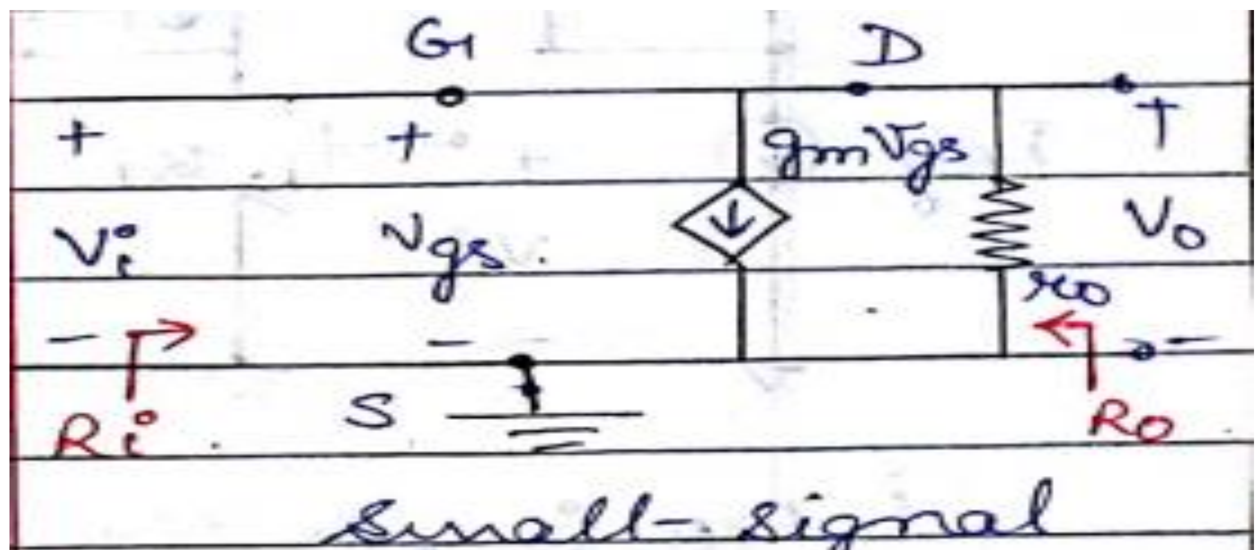
= also called Early Voltage.

Equa. ③ indicates that when channel-length modulation is considered, the saturation values of i_D depends on V_{DS}. Thus for a given V_{GS}, a change ΔV_{DS} yields a corresponding change Δi_D in i_D. So the o/p resistance of current source representing i_D in saturation is no longer infinite.

$$\therefore r_o = \left[\frac{i_D}{V_{DS}}\right]^{-1}_{V_{GS} = \text{constant}} \quad — ④ \qquad \left\{ r_o = \frac{V_{DS}}{i_D} \right\}$$

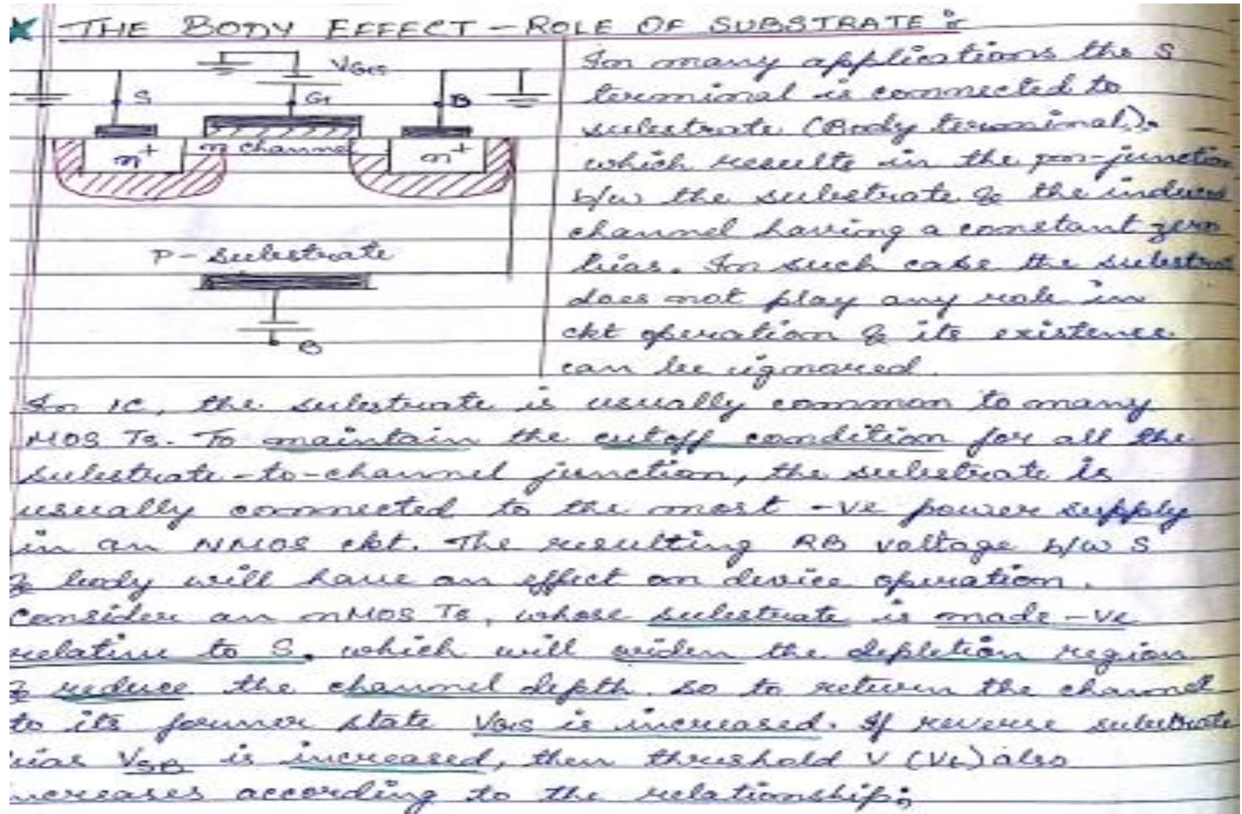


2b. Draw the small signal equivalent model of NMOS by considering r_o and explain.



3a. What is body effect and how it affects threshold voltage?

Ans 3a.



THE BODY EFFECT – ROLE OF SUBSTRATE :

For many applications the S terminal is connected to substrate (Body terminal), which results in the pn-junction b/w the substrate & the induced channel having a constant zero bias. In such case the substrate does not play any role in ckt operation & its existence can be ignored.

In IC, the substrate is usually common to many MOS Ts. To maintain the cutoff condition for all the substrate-to-channel junction, the substrate is usually connected to the most –ve power supply in an NMOS ckt. The resulting RB voltage b/w S & body will have an effect on device operation. Consider an nMOS Ts, whose substrate is made –ve relative to S, which will widen the depletion region & reduce the channel depth. So to return the channel to its former state V_{GS} is increased. If reverse substrate bias V_{SB} is increased, then threshold V (V_t) also increases according to the relationship:

$$V_t = V_{t0} + \gamma\left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right] \quad \text{— (1)}$$

where V_{t0} = threshold voltage for $V_{SB} = 0$.

ϕ_f = physical parameter ; $2\phi_f = 0.6V$ typically

γ = fabrication-process parameter.

$$\gamma = \frac{\sqrt{2qN_A\epsilon_s}}{C_{ox}} \quad \text{— (2)} = \text{body-effect parameter.}$$

$\phi_f = \left(\frac{kT}{q}\right)\ln\left(\frac{N_a}{n_i}\right)$ = Fermi potential of material

where q = $\bar{e}$ charge = 1.6×10^{-19} C.

N_A = doping concentration of p-type substrate

ϵ_s = permittivity of Si = $11.7\epsilon_0 = 11.7 \times 8.854 \times 10^{-14} \approx 1.04 \times 10^{-12}$ F/cm

γ = dimension $\sqrt{V}$, typically $0.4\ V^{1/2}$.

equa (1) is applicable for a p-channel device as well by taking $|V_{SB}|$ & γ = –ve.

& $\gamma = \frac{\sqrt{2qN_D\epsilon_s}}{C_{ox}}$; N_D = doping conc. of n-type substrate

$2\phi_f = 0.75V$ & $\gamma = -0.5V^{1/2}$

equa.(1) indicates; incremental change in V_{SB} gives rise to an incremental change in V_t, which in turn results in an incremental change in i_D even though V_{GS} might have been kept constant. The body voltage controls i_D thus the body acts as another gate for the MOSFET, this phenomenon is known as body effect. The body-effect can cause considerable degradation in ckt performance

Q4. Design the circuit with R_D and R_S where n-MOS transistor operates at V_{DD}=+2.5V, V_{SS}=-2.5V, I_D=0.4mA and V_D=+0.5V. The transistor has V_t=0.7V, μ_nC_{ox}=100µA/V^2, L=1µm, W=32µm and gate is at ground. Neglect the channel length modulation effect.

Ans

$V_{DD} = +2.5V$, i_D, $R_D = 5K\Omega$, V_D, G, D, S, V_S, $R_S = 3.25K\Omega$, i_S, $V_{SS} = -2.5V$

∵ $V_D = +0.5V > V_G$, means nMOS Ts is operating in saturation region. so saturation-region expression of i_D is used to determine value of V_{GS}.

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2$$

∵ $I_D = 0.4mA = 400\mu A$, $\mu_n C_{ox} = 100\mu A/V^2$.

$\frac{W}{L} = \frac{32\mu m}{1\mu m} = 32$ & $V_{GS} - V_t = V_{OV}$

$$\therefore 400\times10^{-6} = \frac{100\times10^{-6}}{2}\times 32 \times V_{OV}^2$$

$\Rightarrow V_{OV}^2 = \frac{4}{16} \Rightarrow V_{OV} = \frac{1}{2} = 0.5V.$

∴ $V_{GS} - V_t = V_{OV} \Rightarrow V_{GS} = V_{OV} + V_t = 0.5 + 0.7 \Rightarrow V_{GS} = 1.2V$.

Figure shows G is at gnd potential, ∴ S must be at $-1.2V$. & the required value of R_S is determined as

$$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-1.2-(-2.5)}{0.4\times10^{-3}} = 3.25K\Omega.$$

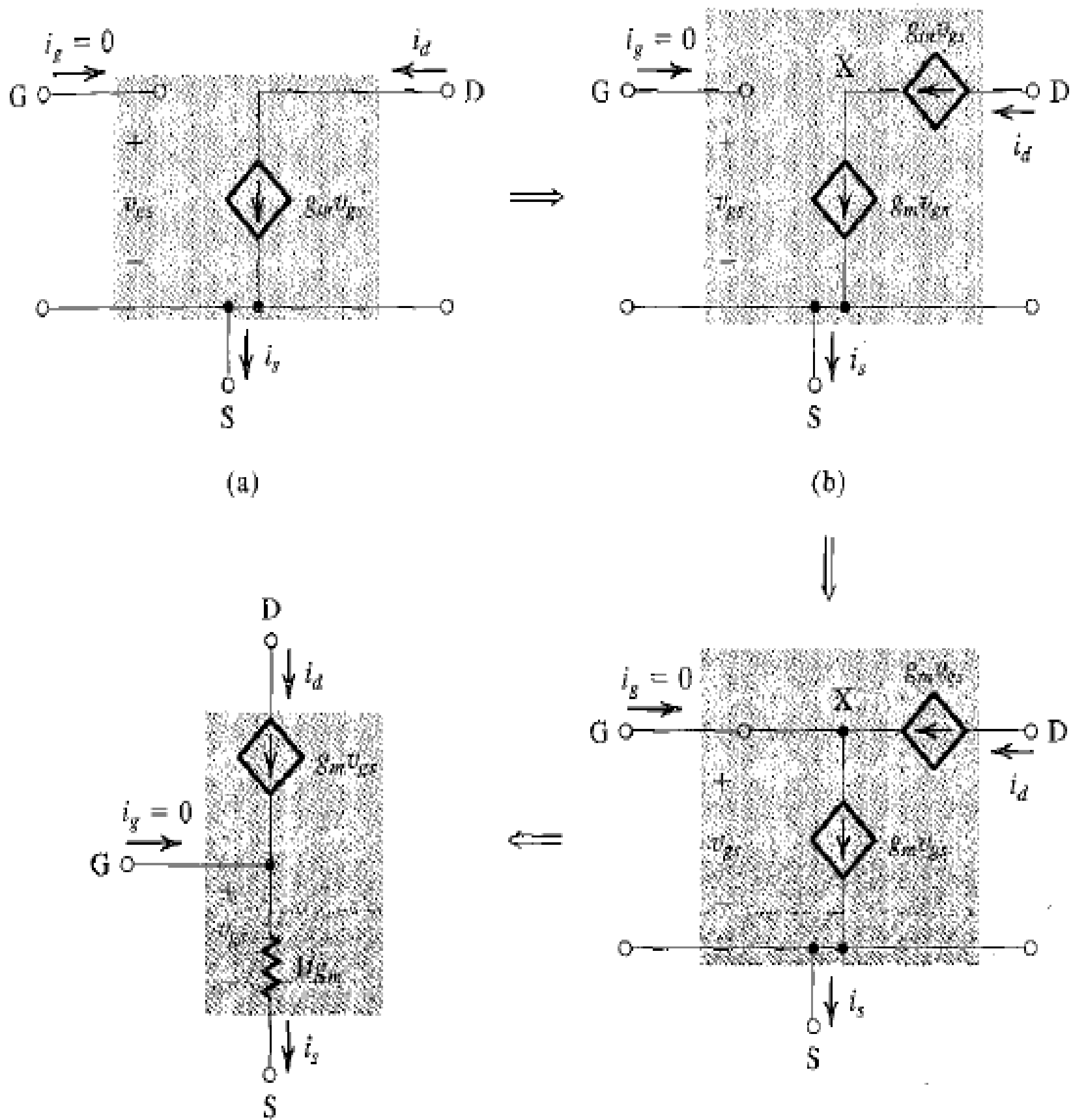
To design the ckt, to establish a dc voltage of +0.5V at

the D, we must select R_D as follows.

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5\,k\Omega$$

5a.Draw the development of the T-equivalent circuit model for the MOSFET.

Ans.



5b. Briefly explain two types of biasing methods in MOS amplifier circuits

Ans

4.5.1 Biasing by Fixing V_{GS}

The most straightforward approach to biasing a MOSFET is to fix its gate-to-source voltage V_{GS} to the value required to provide the desired I_D. This voltage value can be derived from the power supply voltage V_{DD} through the use of an appropriate voltage divider. Alternatively, it can be derived from another suitable reference voltage that might be available in the system. Independent of how the voltage V_{GS} may be generated, this is not a good approach to biasing a MOSFET. To understand the reason for this statement, recall that

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

and note that the values of the threshold voltage V_t, the oxide-capacitance C_{ox}, and (to a lesser extent) the transistor aspect ratio W/L vary widely among devices of supposedly the same size and type. This is certainly the case for discrete devices, in which large spreads in the values of these parameters occur among devices of the same manufacturer's part number. The spread is also large in integrated circuits, especially among devices fabricated on different wafers and certainly between different batches of wafers. Furthermore, both V_t and μ_n depend on temperature, with the result that if we fix the value of V_{GS}, the drain current I_D becomes very much temperature dependent.

4.5.2 Biasing by Fixing V_G and Connecting a Resistance in the Source

An excellent biasing technique for discrete MOSFET circuits consists of fixing the dc voltage at the gate, V_G, and connecting a resistance in the source lead, as shown in Fig. 4.30(a). For this circuit we can write

$$V_G = V_{GS} + R_S I_D \tag{4.46}$$

Now, if V_G is much greater than V_{GS}, I_D will be mostly determined by the values of V_G and R_S. However, even if V_G is not much larger than V_{GS}, resistor R_S provides *negative feedback*, which acts to stabilize the value of the bias current I_D. To see how this comes about consider the case when I_D increases for whatever reason. Equation (4.46) indicates that since V_G is constant, V_{GS} will have to decrease. This in turn results in a decrease in I_D, a change that is opposite to that initially assumed. Thus the action of R_S works to keep I_D as constant as possible. This negative feedback action of R_S gives it the name **degeneration resistance,** a name that we will appreciate much better at a later point in this text.

Figure 4.30(b) provides a graphical illustration of the effectiveness of this biasing scheme. Here we show the i_D–v_{GS} characteristics for two devices that represent the extremes of a batch of MOSFETs. Superimposed on the device characteristics is a straight line that represents the constraint imposed by the bias circuit—namely, Eq. (4.46). The intersection of this straight line with the i_D–v_{GS} characteristic curve provides the coordinates (I_D and V_{GS}) of the bias point. Observe that compared to the case of fixed V_{GS}, here the variability obtained in I_D is much smaller. Also, note that the variability decreases as V_G and R_S are made larger (providing a bias line that is less steep).

6. Derive the expression for transconductance g_m and voltage gain A_v for a common source amplifier with small input signal.

Ans.

Next, consider the situation with the input signal v_{gs} applied. The total instantaneous gate-to-source voltage will be

$$v_{GS} = V_{GS} + v_{gs} \quad (4.56)$$

resulting in a total instantaneous drain current i_D,

$$\begin{aligned} i_D &= \frac{1}{2}k_n'\frac{W}{L}(V_{GS} + v_{gs} - V_t)^2 \\ &= \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_t)^2 + k_n'\frac{W}{L}(V_{GS} - V_t)v_{gs} + \frac{1}{2}k_n'\frac{W}{L}v_{gs}^2 \end{aligned} \quad (4.57)$$

The first term on the right-hand side of Eq. (4.57) can be recognized as the dc bias current I_D (Eq. 4.54). The second term represents a current component that is directly proportional to the input signal v_{gs}. The third term is a current component that is proportional to the square of the input signal. This last component is undesirable because it represents *nonlinear distortion*. To reduce the nonlinear distortion introduced by the MOSFET, the input signal should be kept small so that

$$\frac{1}{2}k_n'\frac{W}{L}v_{gs}^2 \ll k_n'\frac{W}{L}(V_{GS} - V_t)v_{gs}$$

resulting in

$$v_{gs} \ll 2(V_{GS} - V_t) \quad (4.58)$$

or, equivalently,

$$v_{gs} \ll 2V_{OV} \quad (4.59)$$

where V_{OV} is the overdrive voltage at which the transistor is operating.

If this **small-signal condition** is satisfied, we may neglect the last term in Eq. (4.57) and express i_D as

$$i_D \simeq I_D + i_d \quad (4.60)$$

where

$$i_d = k_n'\frac{W}{L}(V_{GS} - V_t)v_{gs}$$

The parameter that relates i_d and v_{gs} is the MOSFET **transconductance** g_m,

$$g_m \equiv \frac{i_d}{v_{gs}} = k_n'\frac{W}{L}(V_{GS} - V_t) \quad (4.61)$$

or in terms of the overdrive voltage V_{OV},

$$g_m = k_n'\frac{W}{L}V_{OV} \quad (4.62)$$

Figure 4.35 presents a graphical interpretation of the small-signal operation of the enhancement MOSFET amplifier. Note that g_m is equal to the slope of the i_D–v_{GS} characteristic at the bias point,

$$g_m \equiv \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{GS} = V_{GS}} \quad (4.63)$$

This is the formal definition of g_m, which can be shown to yield the expressions given in Eqs. (4.61) and (4.62).

4.6.3 The Voltage Gain

Returning to the circuit of Fig. 4.34, we can express the total instantaneous drain voltage v_D as follows:

$$v_D = V_{DD} - R_D i_D$$

Under the small-signal condition, we have

$$v_D = V_{DD} - R_D(I_D + i_d)$$

which can be rewritten as

$$v_D = V_D - R_D i_d$$

Thus the signal component of the drain voltage is

$$v_d = -i_d R_D = -g_m v_{gs} R_D \tag{4.64}$$

which indicates that the voltage gain is given by

$$A_v \equiv \frac{v_d}{v_{gs}} = -g_m R_D \tag{4.65}$$

7a. Explain the operation of MOSFET as a switch

Ans

★ MOSFET AS A SWITCH :-

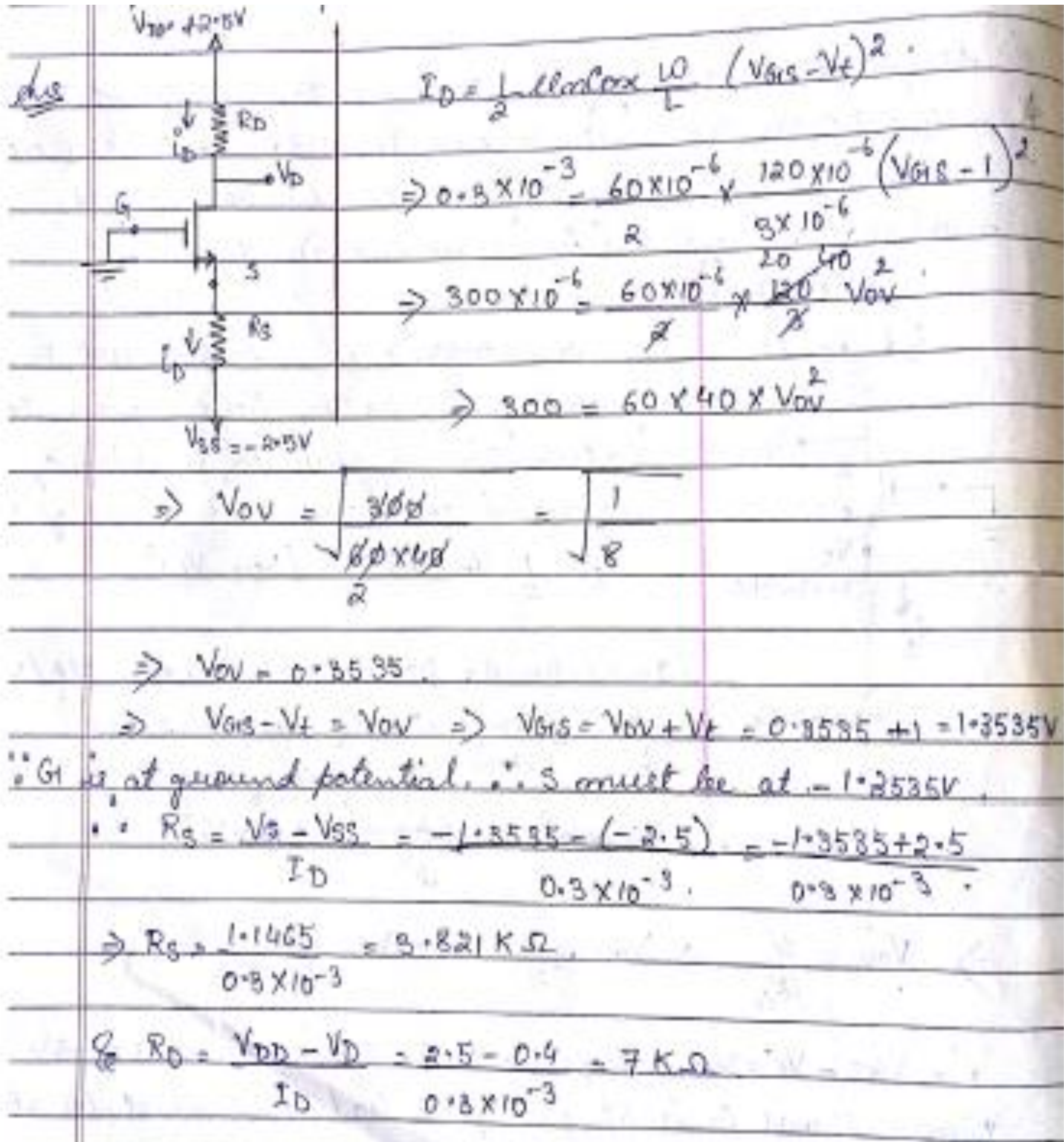
When MOSFET is used as a switch it operates at the extreme points of the transfer characteristics; Device

1) Device = OFF, when $V_I < V_t$. operation within XA with $V_O = V_{DD}$.
2) Device = ON, when $V_I \approx V_{DD}$. operation close to point C $V_O = V_{OC}$ with very small V_O (at C $V_O = V_{OC}$)

∴ Common-source MOS ckt behaves as a inverter ckt. low V level ≈ 0 & high V level ≈ V_{DD}

7b. Design the circuit with R_D and R_S where n-MOS transistor operates at V_{DD}=+2.5V, V_{SS}=-2.5V, I_D=0.3mA and V_D=+0.4V. The transistor has V_t=1V, μ_nC_{ox}=60µA/V^2, W/L=120µm/3µm and gate is at ground. Neglect the channel length modulation effect.

Ans.



Ans

$V_{DD} = +2.5V$, R_D, I_D, V_D, G, S, R_S, I_D, $V_{SS} = -2.5V$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

$$\Rightarrow 0.3\times10^{-3} = \frac{60\times10^{-6}}{2}\times\frac{120\times10^{-6}}{3\times10^{-6}}(V_{GS} - 1)^2$$

$$\Rightarrow 300\times10^{-6} = \frac{60\times10^{-6}}{2}\times\frac{120}{3}V_{ov}^2$$

$$\Rightarrow 300 = 60\times40\times V_{ov}^2$$

$$\Rightarrow V_{ov} = \sqrt{\frac{300}{\frac{60\times40}{2}}} = \sqrt{\frac{1}{8}}$$

$$\Rightarrow V_{ov} = 0.3535$$

$$\Rightarrow V_{GS} - V_t = V_{ov} \Rightarrow V_{GS} = V_{ov} + V_t = 0.3535 + 1 = 1.3535V$$

∵ G is at ground potential, ∴ S must be at $-1.3535V$.

$$\because R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-1.3535 - (-2.5)}{0.3\times10^{-3}} = \frac{-1.3535 + 2.5}{0.3\times10^{-3}}$$

$$\Rightarrow R_S = \frac{1.1465}{0.3\times10^{-3}} = 3.821\,K\Omega$$

$$\&\ R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.4}{0.3\times10^{-3}} = 7\,K\Omega$$