Solutions & Scheme of Evaluation
Internal Assessment Test 1 – March.2019

Sub:	Linear Integrated circuits							Code:	17EC45
Date:	07/03/2019	Duration:	90mins	Max Marks:	50	Sem:	IV	Branch:	ECE(A,B,C,D)

Note: Answer Any Five Questions

Question #		Description	Max Marks
1		**Explain in detail the basic op-amp internal circuit with a neat diagram and also explain input and output voltage ranges.** • circuit diagram – 4M • Explanation – 4M • input and output voltage range – 2M	10 M

BASIC OPERATIONAL AMPLIFIER CIRCUIT

The basic circuit of an operational amplifier is illustrated in Fig. 1-4. *Plus* and *minus* supply voltages ($+V_{CC}$ and $-V_{EE}$) are provided, and the two input terminals are grounded. Transistors Q_1 and Q_2 constitute a *differential amplifier*, which produces a voltage change at the collector of Q_2 when a difference input voltage is applied to the bases of Q_1 and Q_2. Transistor Q_3 operates as an emitter-follower to provide a low output impedance. As illustrated, the *dc* output voltage level at terminal # 6 is

$$V_o = V_{CC} - V_{RC} - V_{BE3}$$

or

$$V_o = V_{CC} - (I_{C2}R_C) - V_{BE} \qquad (1\text{-}1)$$

Assume that Q_1 and Q_2 are *matched transistors*, that is they have equal V_{BE} levels and equal current gains. Then, with both transistor bases at ground level, the emitter currents are equal, and both I_{E1} and I_{E2} flow through the common emitter resistor, R_E. The total emitter current could be calculated as

$$I_{E1} + I_{E2} = \frac{V_{RE}}{R_E}$$

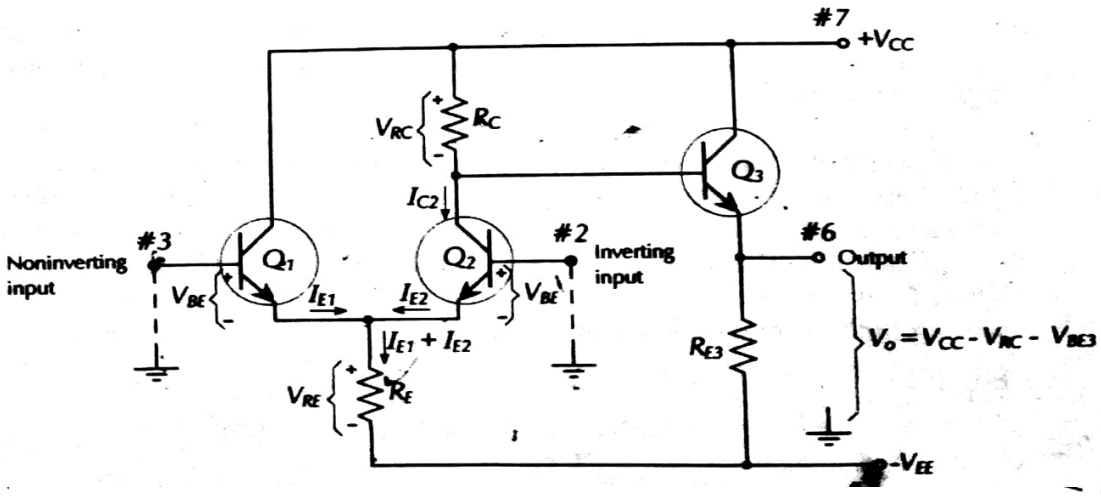
With Q_1 and Q_2 bases grounded,

$$V_{RE} = V_{EE} - V_{BE}$$

so,

$$I_{E1} + I_{E2} = \frac{V_{EE} - V_{BE}}{R_E} \qquad (1\text{-}2)$$

To investigate the circuit operation, assume that $V_{CC} = +10$ V, $V_{EE} = -10$ V, $R_E = 4.7$ kΩ, $R_C = 6.8$ kΩ, and all transistors have $V_{BE} = 0.7$ V.



With both input terminals at ground level,

Eq. 1-2,
$$I_{E1} + I_{E2} = \frac{V_{EE} - V_{BE}}{R_E} = \frac{10\text{ V} - 0.7\text{ V}}{4.7\text{ k}\Omega}$$
$$\approx 2\text{ mA}$$

therefore,
$$I_{E1} = I_{E2} = 1\text{ mA}$$

and
$$I_{C2} \approx I_{E2} \approx 1\text{ mA}$$

Eq. 1-1,
$$V_o = V_{CC} - (I_{C2}R_C) - V_{BE}$$
$$\approx 10\text{ V} - (1\text{ mA} \times 6.8\text{ k}\Omega) - 0.7\text{ V}$$
$$\approx 2.5\text{ V}$$

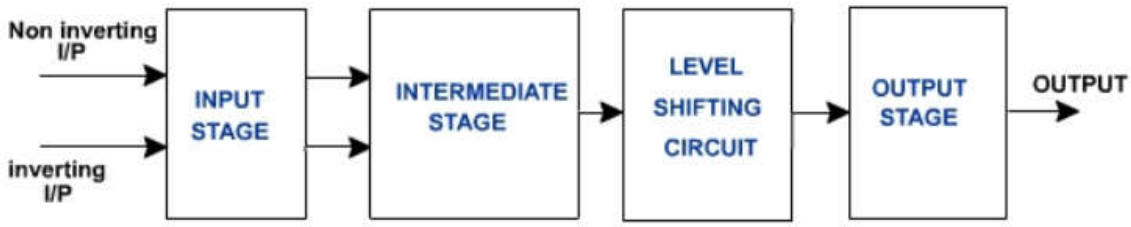
If a positive-going voltage is applied to the noninverting input terminal, Q_1 base is pulled up by the input voltage, and its emitter terminal tends to follow the input signal. Since Q_1 and Q_2 emitters are connected together, the emitter of Q_2 is also pulled up by the positive-going signal at the noninverting input terminal. The base voltage of Q_2 is fixed at ground level so the positive-going movement at its emitter causes a reduction in its base-emitter voltage (V_{BE2}). The result of the reduction in V_{BE2} is that its emitter current is reduced and consequently its collector current is reduced.

For convenience, assume that the positive-going input at the base of Q_1 reduces I_{C2} by 0.2 mA, (i.e., from 1 mA to 0.8 mA). This gives a new level of output voltage.

Eq. 1-1,
$$V_o = V_{CC} - (I_{C2}R_C) - V_{BE}$$
$$= 10\text{ V} - (0.8\text{ mA} \times 6.8\text{ k}\Omega) - 0.7\text{ V}$$
$$\approx 3.9\text{ V}$$

		The output voltage has changed from +2.5 V to +3.9 V, a change of +1.4 V. It is seen that a positive-going signal at the noninverting input terminal has produced a positive-going output voltage. Now consider what occurs when the noninverting terminal is grounded and a positive-going input is applied to the inverting input terminal. In this case, Q_2 base is pulled up, the base-emitter voltage of Q_2 is increased, and that of Q_1 is reduced by a similar amount. This results in an increase in I_{E2} and a consequent increase in I_{C2}. Once again, for convenience, assume that a 0.2 mA change occurs in I_{C2}. Thus, I_{C2} is increased from 1 mA to 1.2 mA by the positive-going voltage at the inverting input terminal. The output voltage can now be calculated as Eq. 1-1, $V_o = V_{CC} - (I_{C2}R_C) - V_{BE}$ $= 10\text{ V} - (1.2\text{ mA} \times 6.8\text{ k}\Omega) - 0.7\text{ V}$ $\approx 1.1\text{ V}$ For $V_s = \pm 15V$ Input range $\pm 13V$ Output swing $\pm 14V$	
2	a)	**741 op-amp is used in a non inverting amplifier with a voltage gain of 50. Calculate the typical output voltage that would result from a common mode input with a peak level of 100 mv.** • CMRR= 31623 - 2M • V0(cm) =158 µV - 3M Soln : Given $A_V = 50$ $V_{i(cm)} = 100mV$ W K T typical value of CMRR for 741 op-amp is 90 dB $(CMRR)_{dB} = 20 \log CMRR$ $CMRR = \text{antilog}\left[\frac{(CMRR)_{dB}}{20}\right] = \text{antilog}\left[\frac{90}{20}\right] = 31,623$ $V_{o(cm)} = \frac{V_{i(cm)}}{CMRR} \cdot A_V = \frac{100m}{31,623} \times 50 = 158\,\mu V$ $V_{o(cm)} = 158\,\mu V$	10 M
	b)	**With a neat block diagram, explain the general stages of an op-amp IC.** • Block diagram – 2M • Explanation – 3M	

BLOCK DIAGRAM REPRESENTATION OF A TYPICAL OPAMP:



[BLOCK DIAGRAM OF A TYPICAL OPAMP]

INPUT STAGE:

1. The input stage is the dual input balanced output differential amplifier.
2. This stage provides most of the voltage gain of the amplifier.
3. It also establishes the input resistance of the OPAMP.

INTERMEDIATE STAGE:

1. The intermediate stage is usually another differential amplifier which is driven by the output of the first stage.
2. In most amplifiers the intermediate stage is dual input and unbalanced (Single ended) output.

LEVEL SHIFTING CIRCUIT:

1. Because direct coupling is used, the DC voltage at the output of the intermediate stage is above ground potential. Therefore, generally the level shifting circuit is used after the intermediate stage to shift the DC level of the output voltage downward to zero voltage with respect to ground.

OUTPUT STAGE:

1. The output stage is usually the emitter follower circuit.
2. The output stage increases the output voltage swing and raises the current supplying capability of the OPAMP.
3. The output stage provides low output resistance.

3 a) **Analyze a voltage follower circuit implemented using a 741 op-amp. Find the minimum and maximum input and output impedances with feedback.** 10 M

AOLmin= 50,000 || Zi= 2 MΩ
AOLmax=2,00,000 || Zo= 75 Ω

- Zin – 2 M
- Zout - 2M

Soln : W.K.T $Z_i = 0.3M\Omega$, $M = 50,000$ (from above)

$Z_{in} = (1 + M\beta) Z_i$

$= [1 + (50,000 \times 1)] 0.3M$ $\because \beta = 1$ for VF

$Z_{in} = 15000\ M\Omega$

Soln : W.K.T $Z_o = 75\Omega$ $M = 2,00,000$ ∵ $\beta = 1$ for VF

$$Z_{out} = \frac{Z_o}{(1+M\beta)} = \frac{75}{(1+200000)}$$

$$\boxed{Z_{out} = 0.004\,\Omega}$$

b) **Design a direct coupled inverting amplifier with gain 50 and output voltage amplitude is to be 2.5 V**

- I1 = 50μA, Vi=50 mv, R3=1KΩ – 1M each
- R1= 1KΩ, R2 = 50KΩ – 1.5M each

Soln : Given : $A_V = 50$ $V_o = 2.5V$

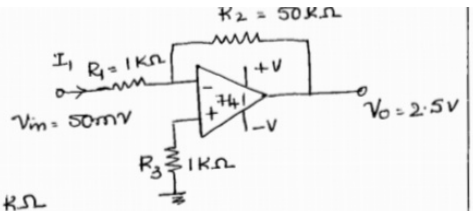
$$A_V = \frac{V_o}{V_{in}} \Rightarrow V_{in} = \frac{V_o}{A_V} = 50\,mV$$

Let $I_1 = 100 I_{Bmax} = 100(500n) = 50\mu A$

$$\therefore V_{in} = \frac{I_1}{R_1} \Rightarrow R_1 = \frac{V_{in}}{I_1} = \frac{50m}{50\mu} = 1K\Omega$$

$$R_2 = \frac{V_o}{I_1} = \frac{2.5}{50\mu} = 50K\Omega$$

$$R_3 = R_1 \| R_2 = 50K \| 1K\Omega = 1K\Omega$$

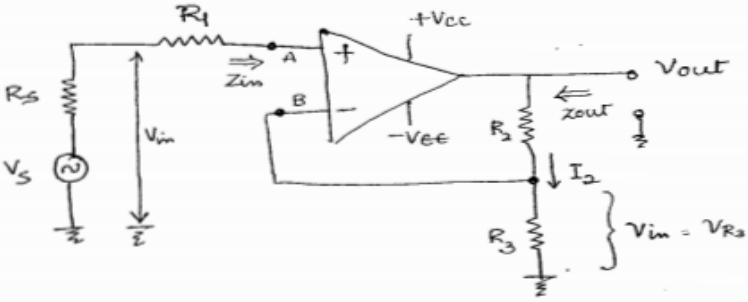


$R_1 = 1K\Omega$
$R_2 = 50K\Omega$
$R_3 = 1K\Omega$

4 a) **Draw an ideal non inverting amplifier using op-amp and derive the expression for its close loop gain.** 10 M

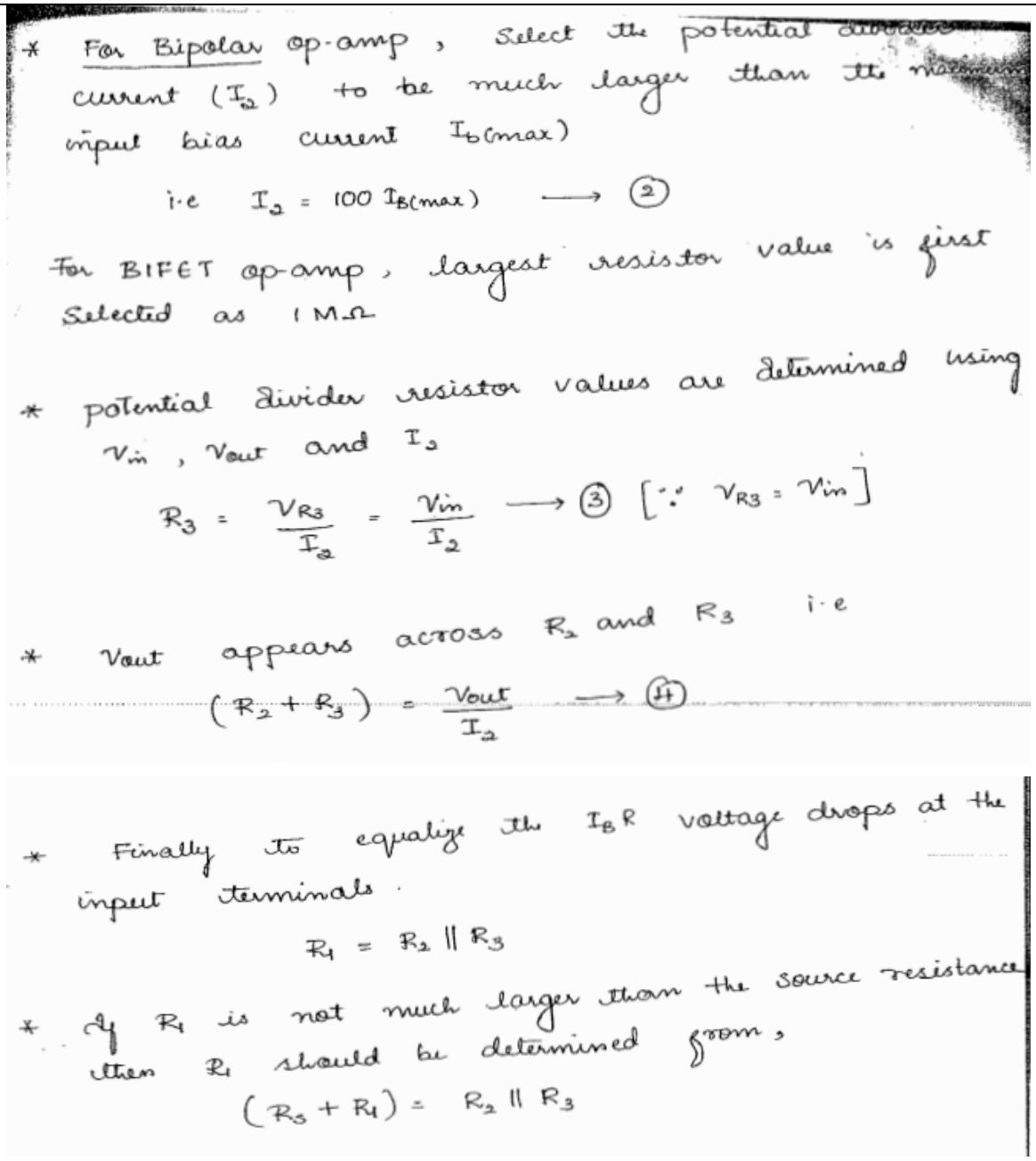
- Circuit diagram – 2M
- Derivation – 3M

Direct Coupled Non-Inverting Amplifier



Design :

* W.K.T the gain of the non-inverting amplifier is given by, $A_V = \left(1 + \frac{R_2}{R_3}\right) = \left(\frac{R_2 + R_3}{R_3}\right)$ ⟶ (1)



b)	**Define i) PSRR ii) slew rate iii) output impedance iv) Input offset voltage v) Input offset current** • Each definition 1M 5 X 1M = 5M		

Power Supply Voltage Rejection (PSRR or SVRR)

Variation in $-V_{EE}$ change the output voltage which has same effect as that of input voltage change. This can be limited using constant current source [Refer note]

* Even with this circuitry, variations in V_{CC} and V_{EE} produces some change in output.
* PSRR is a measure of how effective the op-amp is in dealing with variations in supply voltage.
* If variation of 1V in V_{CC} or V_{EE} causes the output to change by 10mV, then PSRR is 10mV per volt.

$$PSRR = \frac{V_{o(rip)}}{V_{s(rip)}}$$

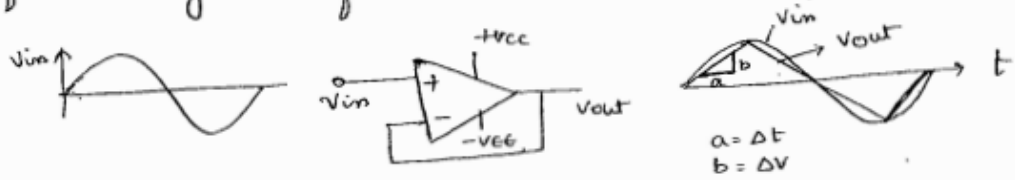
Note: for 741 op-amp, typical value of PSRR = 30μV/V
maximum value of PSRR = 150μV/V

Slew Rate

* Slew rate of an op-amp is the maximum rate at which the output voltage can change.
* When slew rate is too slow, distortion results.

$$SR = \left.\frac{\Delta V_o}{\Delta t}\right|_{max} \text{ V/μs} \quad \Rightarrow \quad t = \frac{\Delta V_o}{S} \text{ sec}$$

* Consider a voltage follower circuit and sine wave is applied as an input to the circuit. A lag wave results because op-amp output simply cannot move fast enough to follow the sine wave input.



Note:
for 741 op-amp, typical slew rate SR = 0.5 V/μsec

Output Impedance

* Like Z_{in}, Z_{out} is also affected by -ve feedback

$$Z_{out} = \frac{Z_o}{(1+M\beta)}$$

where,

Z_o = op-amp o/p impedance without -ve feedback

M = open loop gain of op-amp.

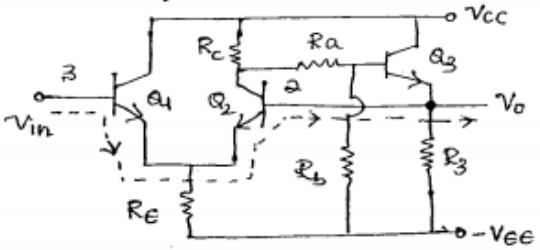
β = feedback factor.

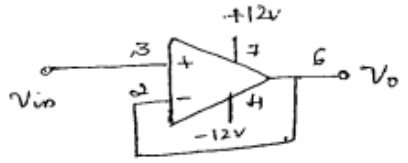
Z_{out} = output impedance of circuit.

Output impedance, typical value $Z_o = 75\Omega$

Input offset and Output offset voltage.

Consider op-amp basic circuit as voltage follower where output follows the input. ($V_o = V_{in}$)





* For a output voltage to be exactly equal to the input voltage, Q_1 and Q_2 needs to be matched.

applying KVL, $V_{in} - V_{BE_1} + V_{BE_2} = V_o$

when Q_1 and Q_2 are matched transistors, V_{BE_1} and V_{BE_2} are equal

and when $V_{in} = 0$, $\boxed{V_{in} = V_o = 0}$

* when Q_1 and Q_2 are not perfectly matched say,

$V_{BE1} = 0.7V$ and $V_{BE2} = 0.6V$, $V_{in} = 0$

$$V_o = 0 - 0.7 + 0.6 = -0.1$$

This unwanted output voltage is known as output offset vltg

To make this $V_o = 0$, the input needs to be raised to $+0.1V$, this is known as Input offset voltage.

** Note : For 741 op-Amp

Input offset voltage : Typical value $V_{ios} = 1mV$
max value $V_{ios} = 5mV$

* ~~either~~ Q_1 and Q_2 transistor are said to be unmatched when Emitter-Base voltages $V_{BE1} \neq V_{BE2}$ and current gain $h_{Fe1} \neq h_{Fe2}$

W.K.T $I_C = \beta \cdot I_B$

* Even though both transistors have equal levels of I_C, I_B of one transistor may vary from the other.

i.e If $I_{B_1} = 1\mu A$, $I_{B_2} = 1.2\mu A$

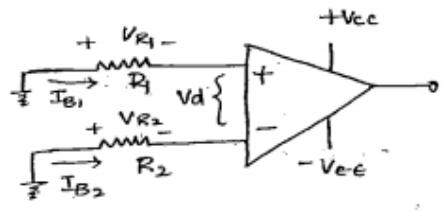
* The difference in these two input current levels is known as input offset current

$$I_{io} = I_B = |I_{B_1} - I_{B_2}|$$

* also,
Even when $R_1 = R_2$, I_{io} produces unequal vltg drop across these resistors and this difference in voltage drop behaves as a differential input voltage which produces an output offset voltage.

Note : For 741 op-amp , Typical value $I_{io} = 20nA$
maximum value $I_{io} = 200nA$

Input Offset Current



$$V_d = V_{R_1} - V_{R_2}$$
$$V_d = I_{B_1} R_1 - I_{B_2} R_2$$

5		**Explain common mode voltage, common mode voltage gain and CMRR for op-amp. Show that** $V_{o(cm)} = \frac{V_{i(cm)}}{CMRR} \; x \; A_{CL}$ **for non inverting amplifier.** • VC, Ac, CMRR – 1M Each • Derivation – 7M	10 M

Common Mode Rejection

Refer again to the basic operational amplifier circuit in Fig. 1-9(b) reproduced in Fig. 2-3 with the feedback connection from output to input deleted. The two input terminals are connected together and both are raised to 1 V above ground level. This is known as a *common mode input*. Note that there is no differential input; both input terminals are at the same potential. So ideally the output should be zero.

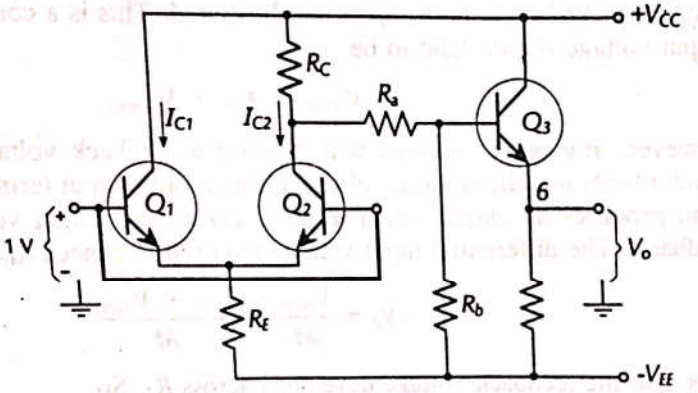


Figure 2-3 Basic op-amp circuit with the two input terminals connected together, and a common mode input voltage applied. The common mode rejection ratio (CMRR) is the open-loop gain divided by the common mode gain. CMRR = M/A_{cm}.

Because the base voltages of Q_1 and Q_2 are raised to 1 V above ground, the voltage drop across emitter resistor R_E is increased by 1 V, and, consequently, I_{C1} and I_{C2} are increased. The increased level of I_{C2} produces an increased voltage drop across resistor R_C, which results in a change in the output voltage at the emitter of Q_3. Similarly, if a -1 V common mode input is applied, I_{C2} falls, and again a change is produced at the circuit output. So, as well as the open-loop (differential input) gain M, each op-amp has a *common mode voltage gain* A_{cm}. The common mode gain is the output voltage change due to the common mode input divided by the common mode input voltage.

$$A_{cm} = \frac{V_{o(cm)}}{V_{i(cm)}}$$

The above discussion refers to the basic operational amplifier circuit. A practical operational amplifier has additional circuitry, such as the constant current tail in Fig. 1-5(a), to minimize the effects of common mode inputs. However, even with such circuitry, common mode signals still have some effect on the output. The success of the op-amp in rejecting common mode inputs is defined in the *common mode rejection ratio (CMRR)*. This is the ratio of the open-loop gain M to the common mode gain A_{cm}.

$$CMRR = \frac{M}{A_{cm}} \tag{2-1}$$

The *CMRR* is usually expressed as a decibel quantity on the op-amp data sheet.

$$CMRR = 20 \log \frac{M}{A_{cm}} \text{ dB} \tag{2-2}$$

The effect of op-amp common mode gain is modified by feedback, just as the open-loop differential gain is modified by feedback to give a closed-loop gain. Consider the noninverting amplifier circuit in Fig. 2-4. With the input terminal grounded, the circuit output should also be at ground level. Now suppose a sine wave signal is picked up at both inputs, as illustrated. This is a common mode input. The output voltage should tend to be

$$V_{o(cm)} = A_{cm} \times V_{i(com)}$$

However, any output voltage will produce a feedback voltage across resistor R_2, which results in a differential voltage at the op-amp input terminals. The differential input produces an output which tends to cancel the output voltage that caused the feedback. The differential input voltage required to cancel $V_{o(cm)}$ is,

$$V_d = \frac{V_{o(cm)}}{M} = \frac{A_{cm} \times V_{i(cm)}}{M}$$

V_d is also the feedback voltage developed across R_2. So,

$$V_d = \frac{V_{o(cm)} \times R_2}{R_1 + R_2}$$

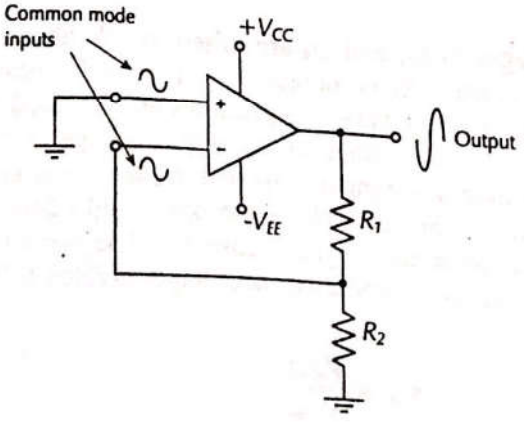


Figure 2-4 A common mode input voltage appears at both input terminals. It is amplified by the common mode gain, but the gain is affected by negative feedback.

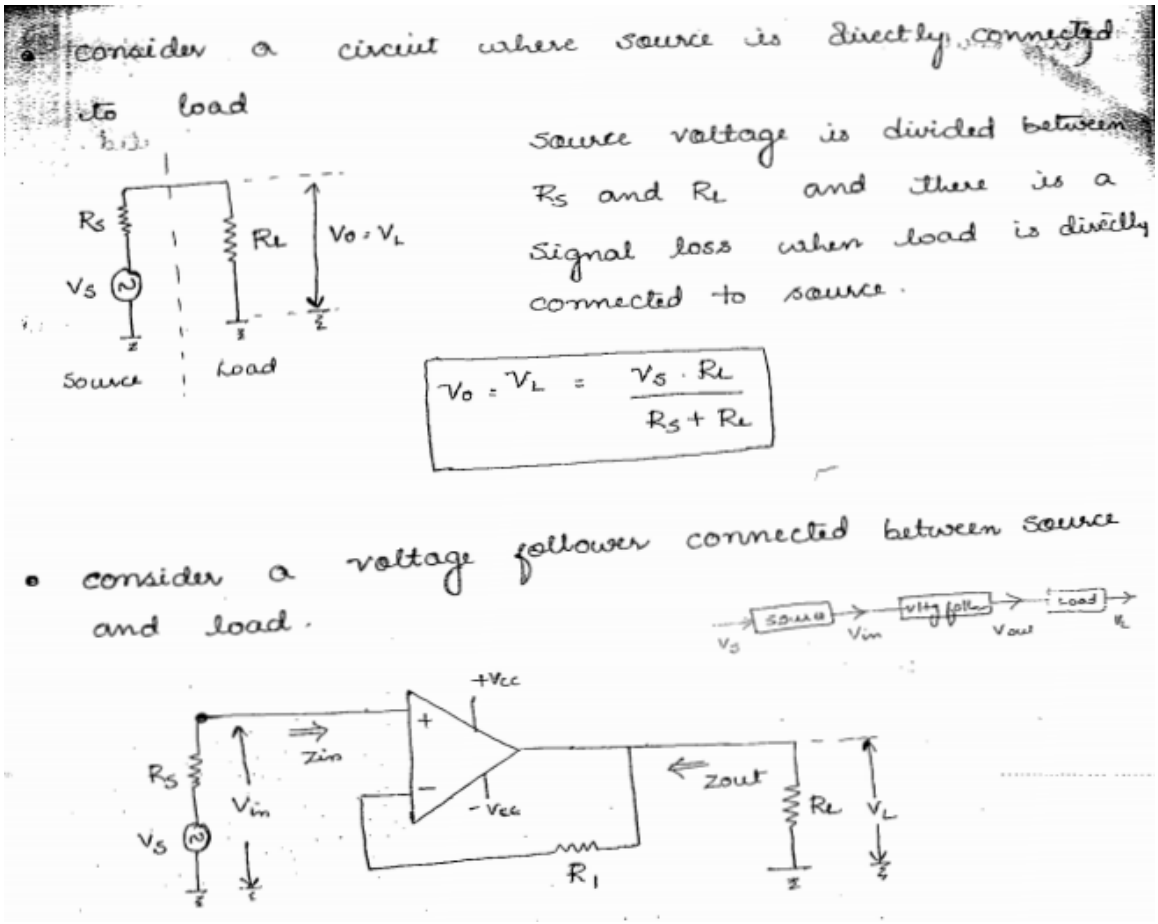
or, $$\frac{V_{o(cm)} \times R_2}{R_1 + R_2} = \frac{A_{cm} \times V_{i(cm)}}{M}$$

giving, $$V_{o(cm)} = \frac{A_{cm} V_{i(cm)}}{M} \times \frac{R_1 + R_2}{R_2}$$

or, $$V_{o(cm)} = \frac{V_{i(cm)}}{CMRR} \times A_v \qquad (2\text{-}3)$$

6 a) **Explain how loading effect can be reduced using voltage follower.** 10 M

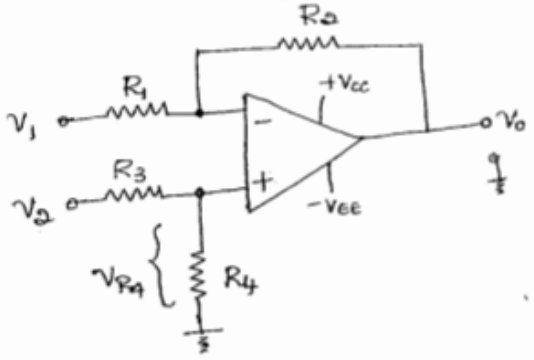
- Explanation with help of diagram – 4M



		* As R_s is much smaller than Z_{in}, there will be no significant loss in signal and all V_{in} appears at input terminal. $V_{in} = \frac{V_s Z_{in}}{R_s + Z_{in}}$ when $Z_{in} = Z_i[1+M]$ * actual output of op-amp is, $V_{out} = V_{in}\left[1 - \frac{1}{M}\right] \Rightarrow V_{out} \approx V_{in}$ [as $\frac{1}{M}$ is less] * As R_L is much greater than Z_{out}, entire output of op-amp is obtained across R_L i.e $V_L = V_{out}$ thus there is no any signal loss. $V_L = \frac{V_{out} \cdot R_L}{R_L + Z_{out}}$ where $Z_{out} = \frac{Z_o}{[1+M]}$ 29. (as Z_{out} is less) $V_L = V_{out}$ $\Rightarrow V_{out} = V_{in}$, loading effect is eliminated.	
b)	**Sketch an op-amp directly coupled difference amplifier circuit. Derive an equation for the output voltage and explain the operation.** • Circuit diagram – 2M • derivation -2M • explanation – 2M		

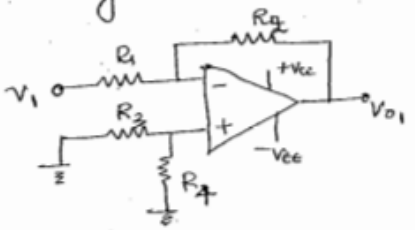
Difference Amplifier

Difference Amplifier amplifies the difference between two input signals. It has 2 inputs connected at both inverting as well as non-inverting terminal



the analysis of the above circuit can be done by using superposition theorem.

case i) when input at non inverting terminal is grounded i.e $V_2 = 0$ and V_1 is acting.

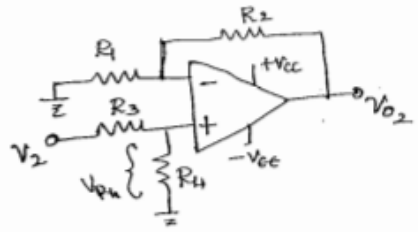


* The circuit behaves like typical inverting amplifier.

$\therefore$ gain $A_V = -\frac{R_2}{R_1}$

$$V_{o1} = A_V \cdot V_1 = -\frac{R_2}{R_1} V_1 \quad \rightarrow (1)$$

case ii) when input at inverting terminal is grounded i.e $V_1 = 0$ and V_2 is acting.

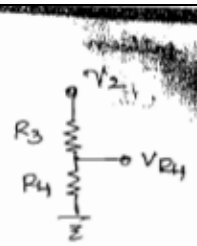


* The circuit is simply a non inverting amplifier.

$\therefore$ gain $A_V = 1 + \frac{R_2}{R_1}$

$V_{02} = A_V \cdot V_{R4}$ ⟶ (2)

where $V_{R4} = \frac{V_2 \cdot R_4}{R_3 + R_4}$ ⟶ (3)



$\therefore V_{02} = \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right) \cdot V_2$ ⟶ (4)

when $R_3 = R_1$, $R_4 = R_2$, eqⁿ (4) reduces to

$V_{02} = \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_2}{R_1 + R_2}\right) V_2$

$\boxed{V_{02} = \frac{R_2}{R_1} \cdot V_2}$ ⟶ (5)

* combining eqⁿ (1) & (3) gives,

$V_0 = V_{01} + V_{02} = -\frac{R_2}{R_1} V_1 + \frac{R_2}{R_1} V_2$

$\boxed{V_0 = +\frac{R_2}{R_1}[V_2 - V_1]}$ ⟶ (6)

If $R_2 = R_1$, $\boxed{V_0 = [V_2 - V_1]}$ ⟶ (7)

Thus the output voltage is the difference between two input voltages.

* when $R_2 > R_1$, O/P is amplified version of input difference.

7	a)	**A load resistance of 22 kΩ is to be connecting to a source of 1.5 V with Source resistance of 56 kΩ. Calculate the load voltage if Load is directly connected to source.** • VL – 2M (7a) $V_L = \frac{V_S \times R_L}{R_S + R_L} = \frac{1.5 \times 22K}{56K + 22K} = 0.423\,V$	10 M
	b)	**Load is connected through voltage follower using op-amp 741. with Zo = 75Ω, Zin = 2 MΩ and AoL = 2x105**	

- Vi, Vo, Zout, VL – each 2M