1. Sketch and Explain high Zin capacitor coupled voltage follower with necessary design steps and show that the input impedance is very high as compared to capacitor coupled voltage follower.

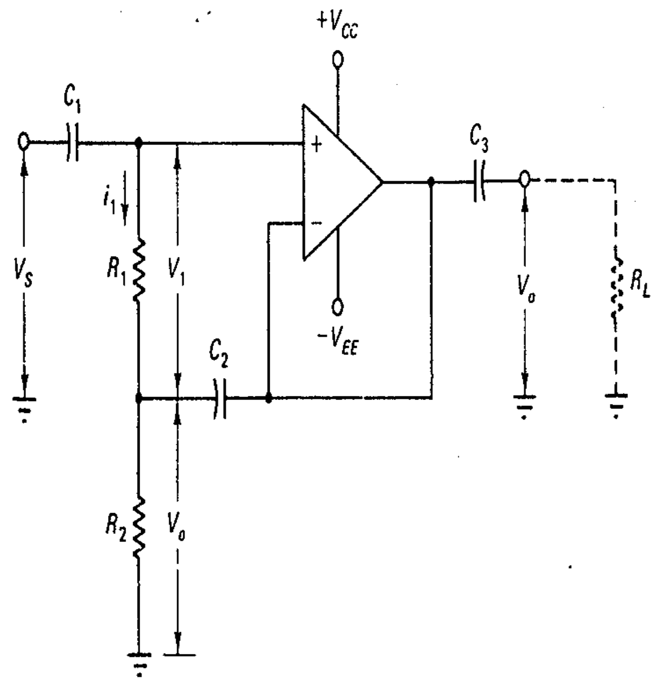


Figure High input impedance capacitor-coupled voltage follower. Feedback via C_2 to the junction of R_1 and R_2 gives an input impedance of $Z_{in} = (1 + M)R_1$.

* The I/p Impedance of the capacitor-coupled voltage follower is set by the value of resistor R_1. This gives a much smaller I/p Impedance than the direct coupled voltage follower.

* Fig ① shows a method by which the I/p Impedance of the capacitor-coupled voltage follower can be substantially increased.

* Capacitor C_2 couples the circuit o/p voltage to the junction of resistors R_1 & R_2.

  C_2 behaves as an ac short circuit. so that 'V_0' is developed across R_2.

* Applying KVL from source, R_1 & R_2,

$$V_S - V_1 - V_0 = 0.$$

The voltage across R_1 is V_1 & is given by

$$\boxed{V_1 = V_S - V_0} \rightarrow ①$$

WKT open-loop gain is given by $M = \frac{V_0}{V_1}$

$$\boxed{V_0 = MV_1} \rightarrow ②$$

Sub eq ② in eq ①, we get

$$V_1 = V_S - MV_1$$

$$MV_1 + V_1 = V_S.$$

$$V_1(1+M) = V_S$$

$$\boxed{V_1 = \frac{V_S}{(1+M)}} \rightarrow ③$$

* The current i_1 is given by :

$$\boxed{i_1 = \frac{V_1}{R_1}} \rightarrow ④$$

sub eq ③ in eq ④, we get

$$\boxed{i_1 = \frac{V_s}{(1+M) R_1}} \rightarrow ⑤$$

* I/P resistance

$$\boxed{Z_{in} = \frac{V_s}{i_1}} \rightarrow ⑥$$

sub eq ⑤ in eq ⑥, we get

$$Z_{in} = \frac{V_s}{\frac{V_s}{(1+M)R_1}}$$

$$\boxed{Z_{in} = (1+M)R_1} \rightarrow ⑦$$

Since open-loop gain 'M' is very high, this nodifies the ckt has very high I/P Impedance.

But if stray capacitance b/w the I/P & ground resent, then I/P Impedance reduces.

Design steps :-

$$R_{1(max)} = \frac{0.1 V_{BE}}{I_{B(max)}}$$

) $R_{1(max)}$ is split into two equal resistors R_1 & R_2

$$\therefore R_1 = R_2 = \frac{R_{1(max)}}{2}$$

3) $\therefore C_2 = \frac{1}{2\pi f_1 \left(\frac{R_2}{10}\right)}$

4) $\boxed{C_1 = C_2}$

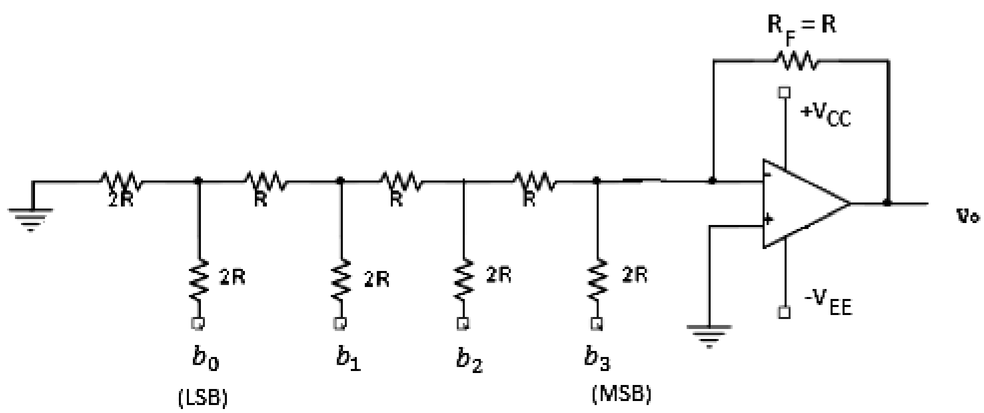
5) $C_3 = \frac{1}{2\pi f_1 R_L}$

6) $Z_{in} = (1+M)R_1$

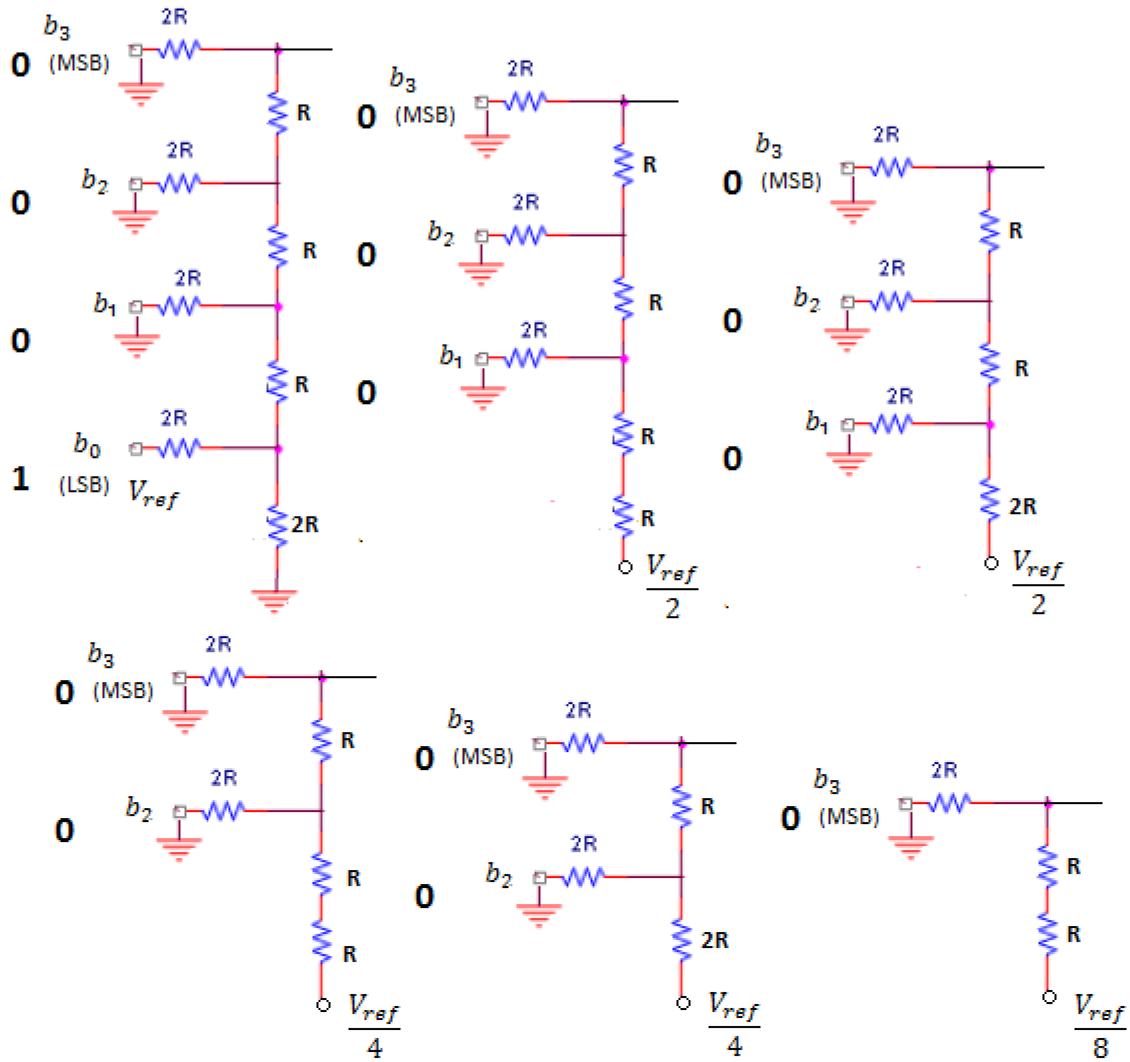
2) Explain the working of R-2R network DAC and derive expression for output voltage.

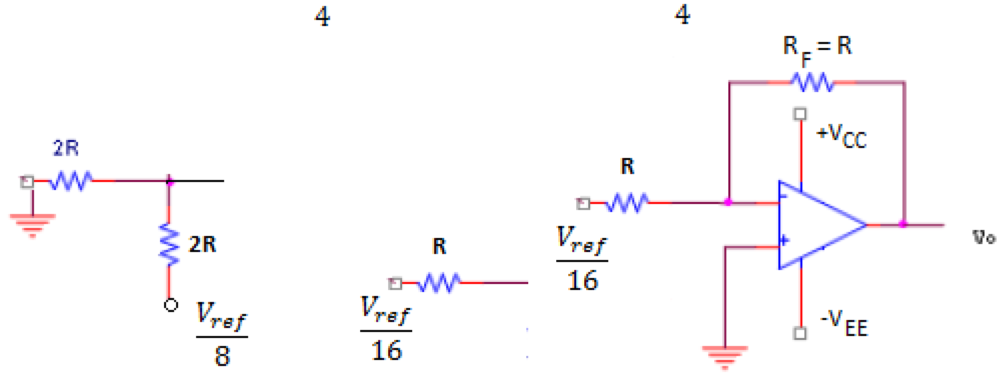
R-2R LADDER:

1. Wide ranges of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC, Here only two values of resistors are required. The typical value of 'R' range from 2.5KΩ to 10KΩ.
2. Consider a 4-bit DAC as shown in figure below, where b_3 , b_2 , b_1 , b_0 are the switches



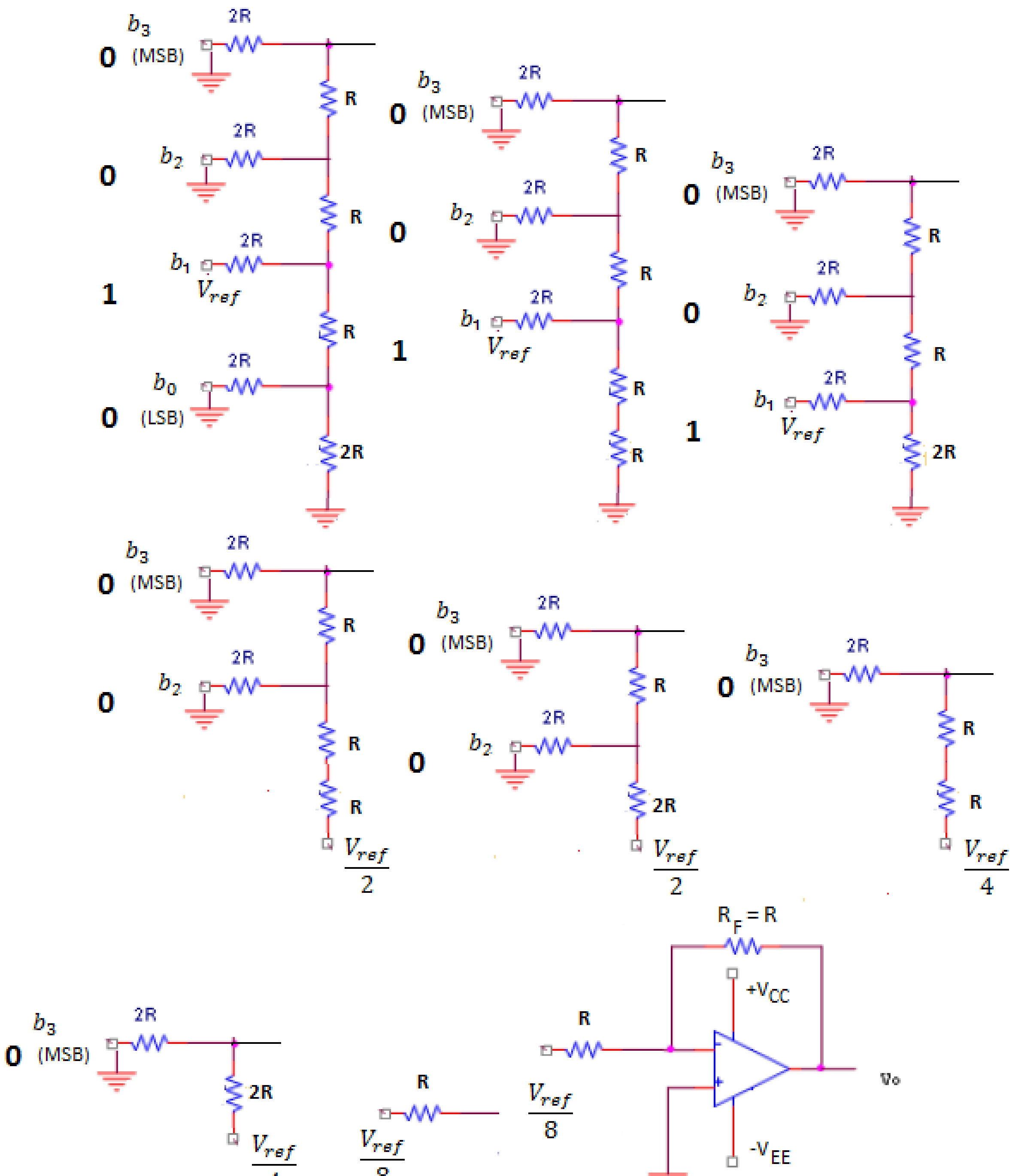
3. When $b_3 b_2 b_1 b_0 = 0001$





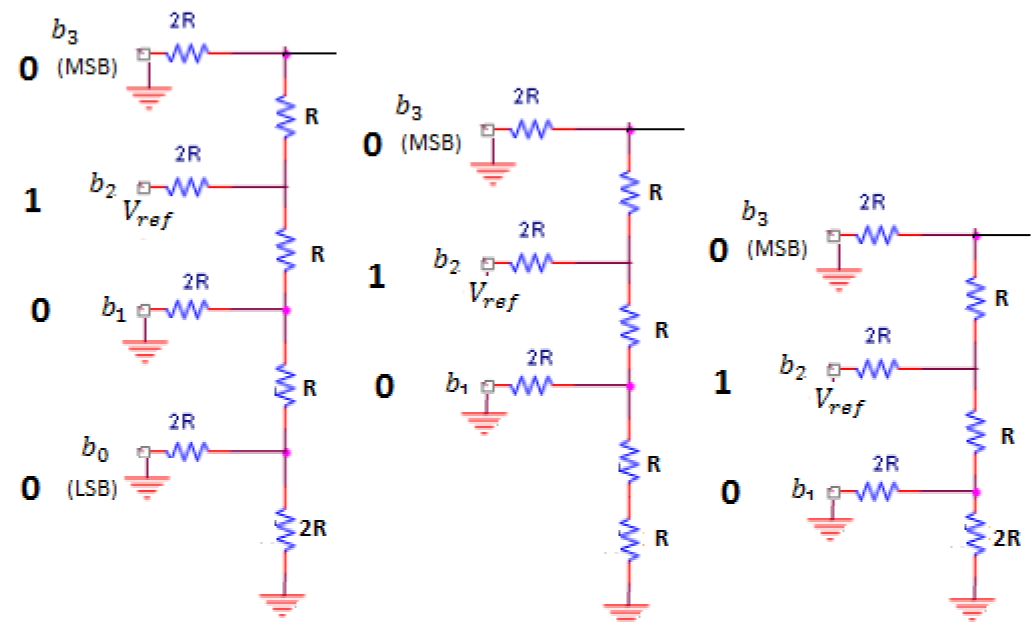
$$V_0 = -\frac{R_f}{R}\left(\frac{V_{ref}}{16}\right)$$

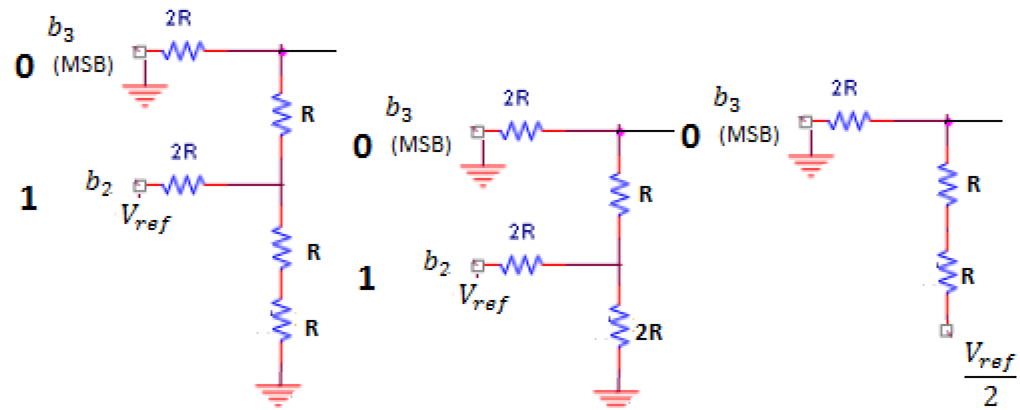
4. When $b_3 b_2 b_1 b_0 = 0010$

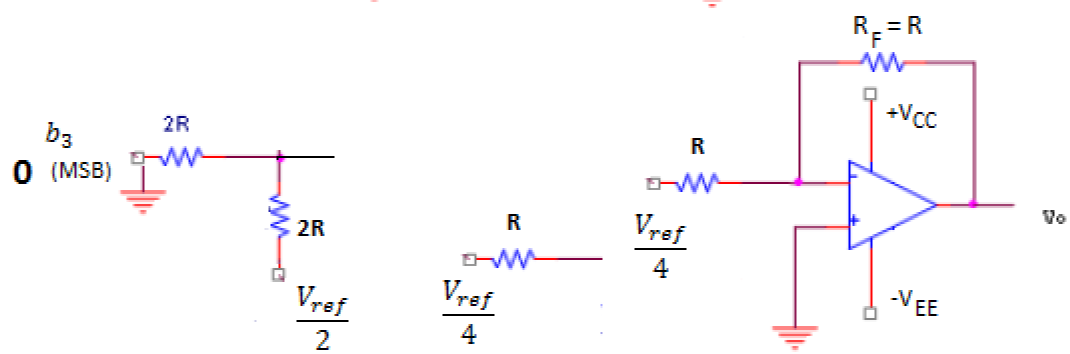


$V_0 = -\frac{R_f}{R}\left(\frac{V_{ref}}{8}\right)$

5. When $b_3 b_2 b_1 b_0 = 0100$

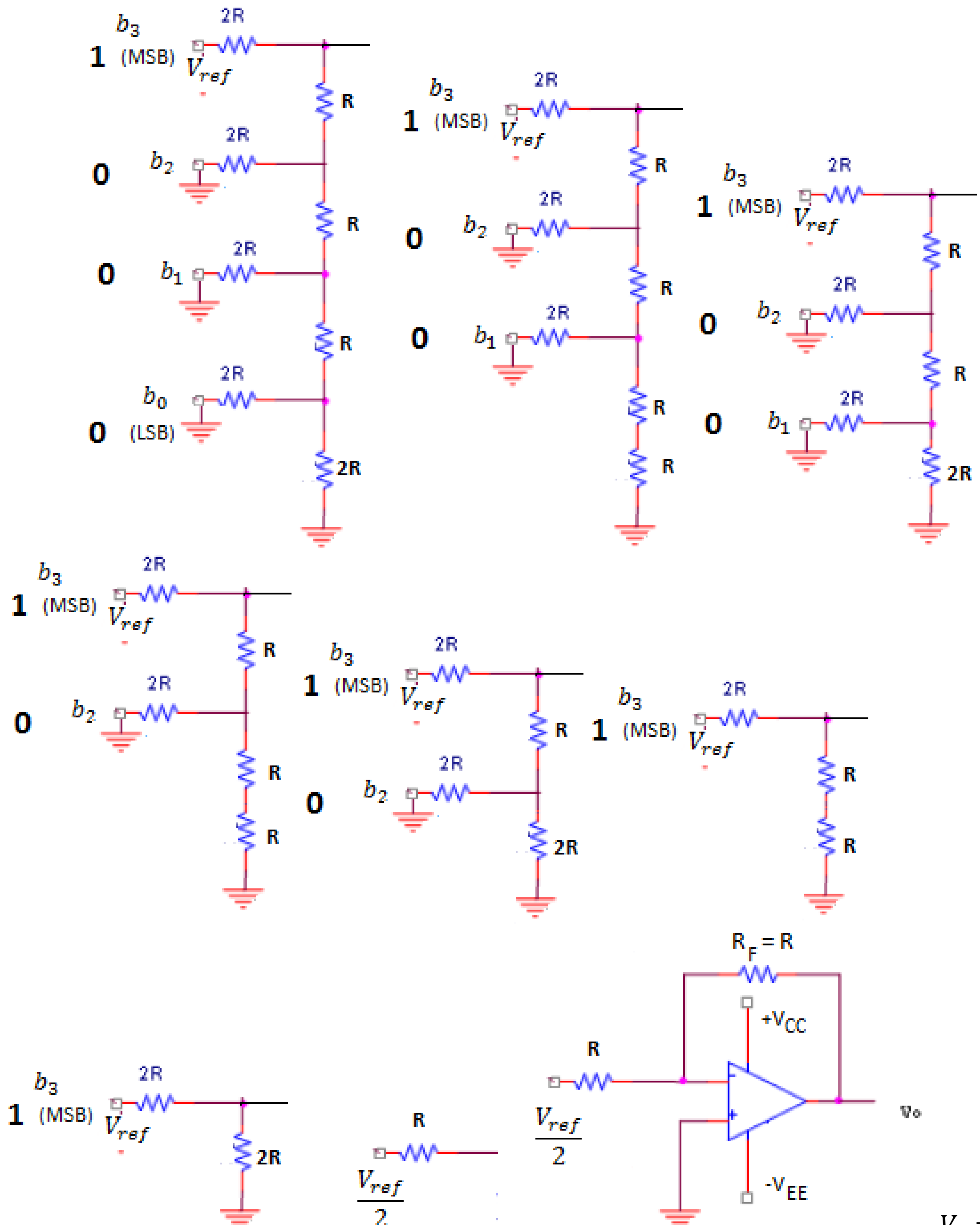






$V_0 = -\frac{R_f}{R}\left(\frac{V_{ref}}{4}\right)$

6. When $b_3 b_2 b_1 b_0 = 1000$



$$V_0 = -\frac{R_f}{R}\left(\frac{V_{ref}}{2}\right)$$

Hence the output can be represented as

$$V_0 = -\frac{R_f}{R} V_{ref} \left(\frac{b_3}{2} + \frac{b_2}{4} + \frac{b_1}{8} + \frac{b_0}{16}\right)$$

3) What are the advantages of precision rectifier over ordinary rectifier? Discuss the operation of full wave rectifier circuit using bipolar op-amp.

The advantages of precision rectifier are

(a) No diode voltage drop between input and output

(b) The ability to rectify very small voltages (less than 0.7V)

(c) Amplification, if required

(d) low output impedance

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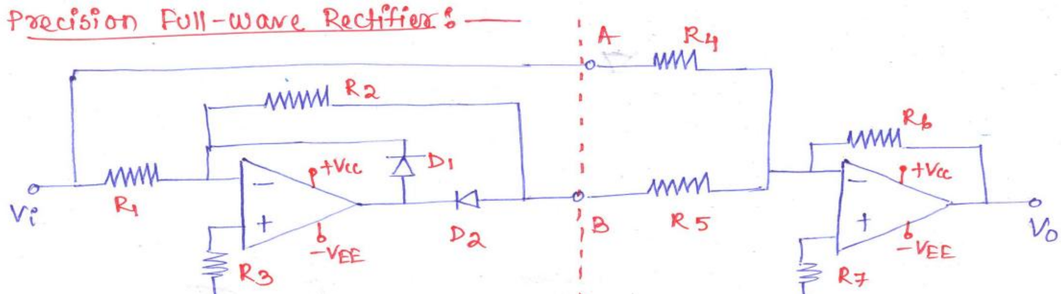
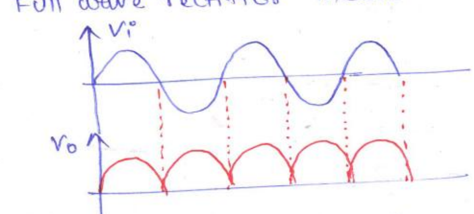
Precision Full-wave Rectifier :—

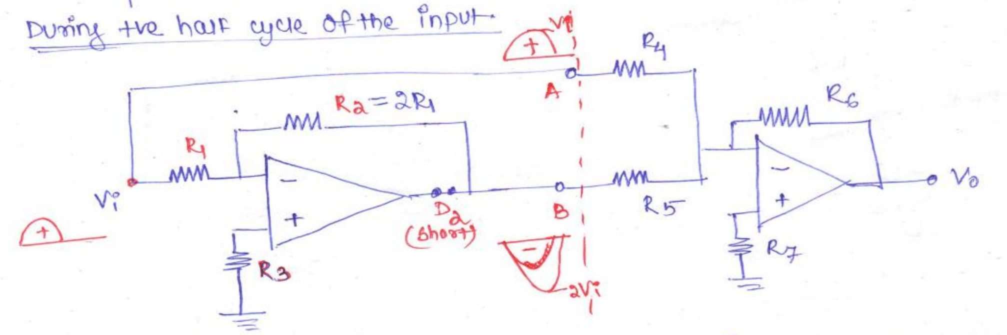


← Precision Rectifier → ← Summing amplifier →

Full wave rectifier means



During +ve half cycle of the input



~~$V_B = -\frac{R_2}{R_1} V_i$~~

~~If $R_2 = R_1$, $V_B =$~~

$$V_o = -\frac{R_6}{R_4} V_A - \frac{R_6}{R_5} V_B$$

If $R_4 = R_5$

$$V_o = -\frac{R_6}{R_4}(V_A + V_B)$$

If $R_4 = R_6$, $V_o = -(V_A + V_B)$ —(

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