CMR INSTITUTE OF TECHNOLOGY

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Internal Assesment Test - II

Sub:	VLSI Design							Code:	15EC63
Date:	16 / 04/ 2019	Duration:	90 mins	Max Marks:	50	Sem:	6th	Branch:	ECE(A, B, & C)

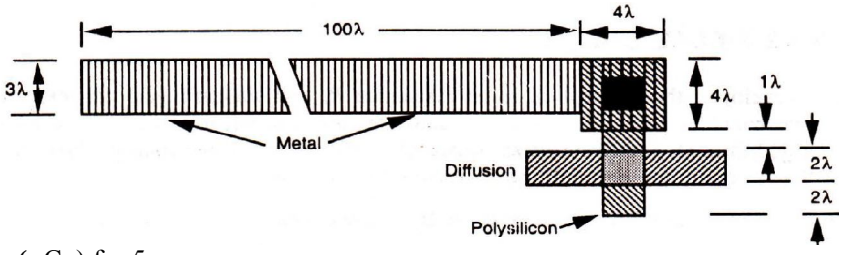
Answer any FIVE full Questions

		Marks	OBE CO	OBE RBT
1.	Compare Bipolar technology with CMOS technology and also explain the n-Well BiCMOS fabrication indicating the additional steps required to fabricate bipolar devices.	[10]	CO1	L1
2.	Explain the fabrication process of nMOS enhancement mode transistor with neat diagrams.	[10]	CO1	L2
3.	Draw the Stick Diagram for the following using nMOS and CMOS Logic: a) $y = \overline{A + B + C}$, b) 2 input NAND Gate	[10]	CO2	L1
4	Realize the boolean expression $y = \overline{a(b + cd)}$ using nMOS and CMOS technology. Also draw the stick and layout diagram of the same in nMOS technology.	[10]	CO2	L3
5.	What are λ-based design rules? List and explain the λ-based design rules for wires and transistors.	[10]	CO2	L1
6.	Derive the expression to calculate total delay of cascaded inverters while driving the large capacitive load.	[10]	CO2	L2
7.	Obtain the scaling factors for the following parameters i) Maximum operating frequency, ii) Channel resistance, iii) Gate capacitance per unit area, iv) Switching energy, v) Gate area	[10]	CO2	L2

PTO

PTO

8.	Calculate the area capacitance of the following structure in terms of standard unit of capacitance (□Cg) for 5 μm process Given: Relative capacitance of Metal1 to substrate: 0.075; Polysilicon to substrate: 0.1; Gate to channel capacitance: 1	[10]	CO1	L3



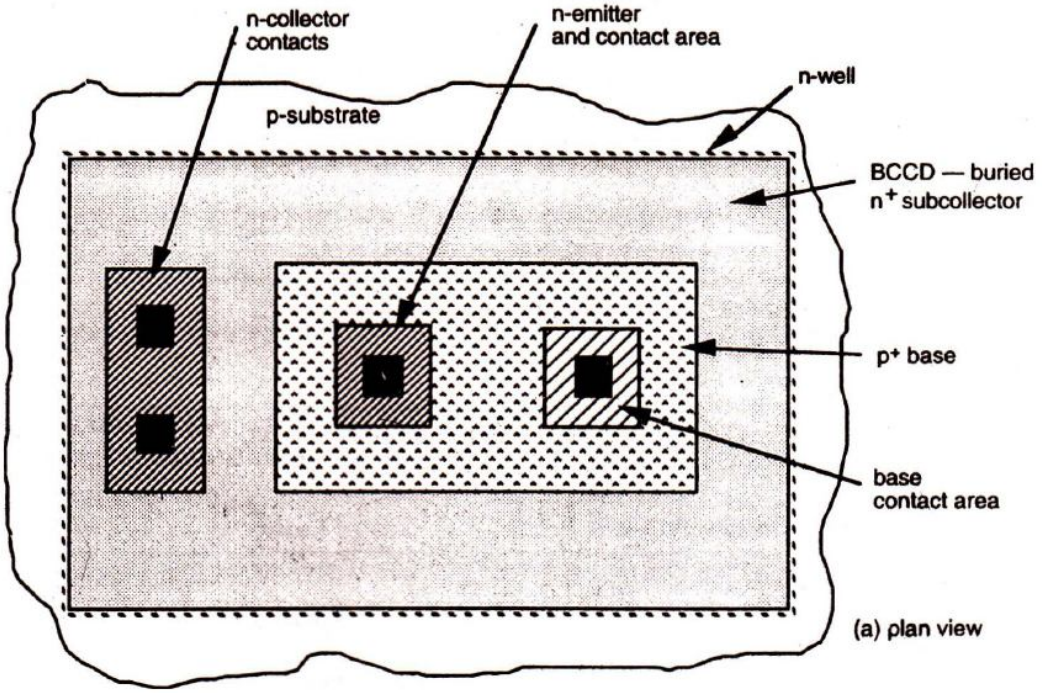
1 Compare Bipolar technology with CMOS technology and also explain the n-Well BiCMOS fabrication indicating the additional steps required to fabricate bipolar devices.

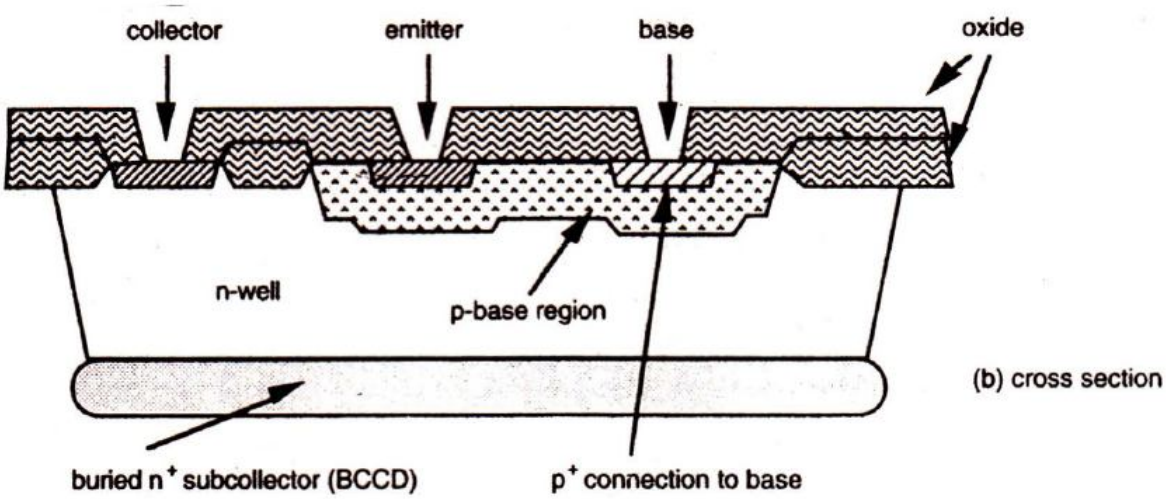
Following table comparison between CMOS and BICMOS technology:

CMOS technology	*Bipolar technology*
• Low static power dissipation	• High power dissipation
• High input impedance (low drive current)	• Low input impedance (high drive current)
• Scalable threshold voltage	
• High noise margin	• Low voltage swing logic
• High packing density	• Low packing density
• High delay sensitivity to load (fan-out limitations)	• Low delay sensitivity to load
• Low output drive current	• High output drive current
• Low g_m ($g_m \alpha V_{in}$)	• High g_m ($g_m \alpha e^{V_{in}}$)
	• High f_t at low currents
• Bidirectional capability (drain and source are interchangeable)	• Essentially unidirectional
• A near ideal switching device	

4 Marks

Following diagrams shows the top view and cross sectional view of Bipolar transistor





The npn transistor is formed in an n-well and the additional p^+ base region is located in the well to form the p-base region of the transistor. The second additional layer-the buried n^+ subcollector (BCCD) is added to reduce the n-well (collector) resistance and thus improve the quality of the bipolar transistor.

2 Marks

The following table lists the additional masks needed to fabricate bipolar devices along with masks required to fabricate CMOS circuit.

n-well BiCMOS fabrication process steps

Single poly. single metal CMOS	*Additional steps for bipolar devices*
• Form n-well	
	• Form buried n^+ layer (BCCD)
• Delineate active areas	
• Channel stop	
	• Form deep n^+ collector
• Threshold V_t adjustment	
• Delineate poly./gate areas	
• Form n^+ active areas	
• Form p^+ active areas	
	• Form p^+ base for bipolars
• Define contacts	
• Delineate the metal areas	

4 Marks

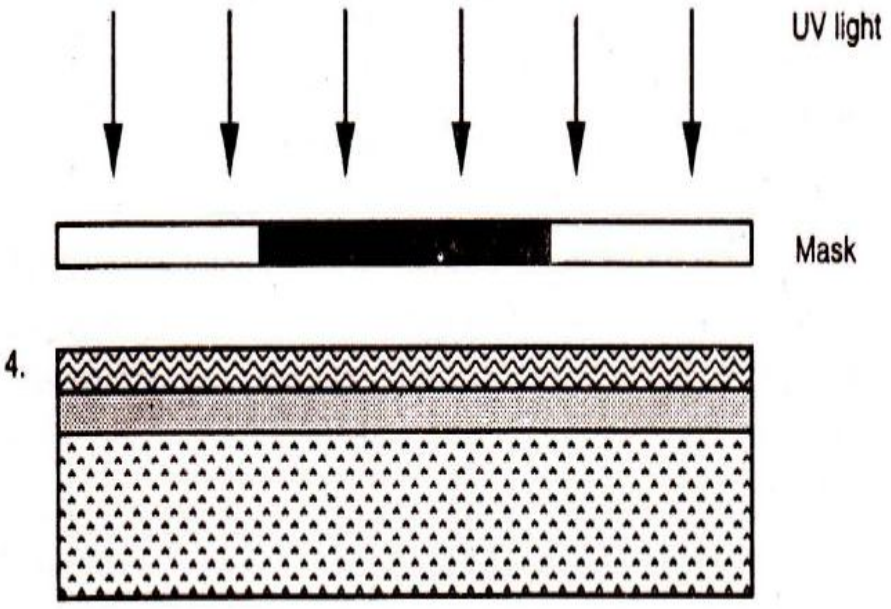
2 Explain the fabrication process of nMOS enhancement mode transistor with neat diagrams.

The fabrication process of nMOS enhancement mode transistor is as follows:

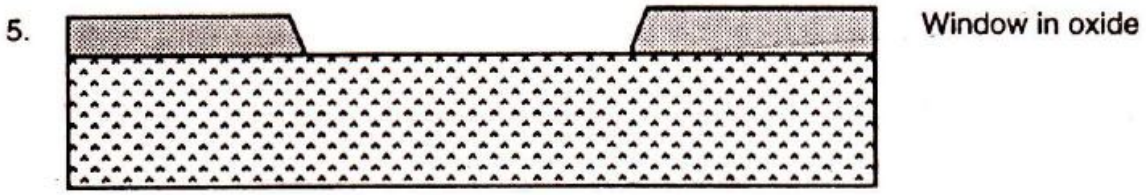
Processing is carried out on a thin wafer cut from a single crystal of silicon of high purity into which the required p-impurities are introduced as the crystal is grown. Such wafers are typically 75-150mm in diameter, 0.4mm thick, doped with boron (concentrations of 10^{15} to 10^{16} / cm^3) and resistivity 25 Ω-cm to 2 Ω-cm

A layer of silicon dioxide (Si02), typically 1 µm thick, is grown all over the surface of the wafer to protect the surface, act as a barrier to dopants during processing, and provide a generally insulating substrate on to which other layers may be deposited and patterned.

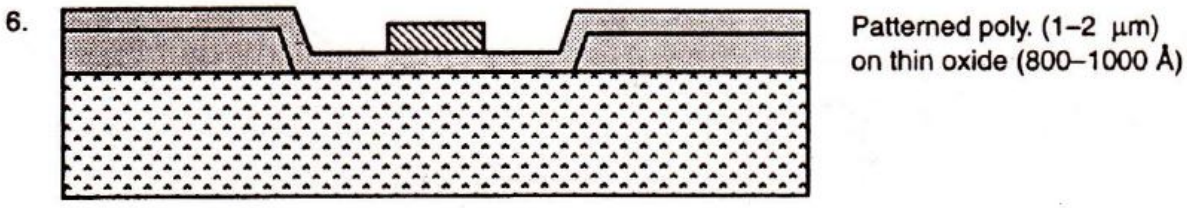
The surface is now covered with a photoresist which is deposited onto the wafer and spun to achieve an even distribution of the required thickness.



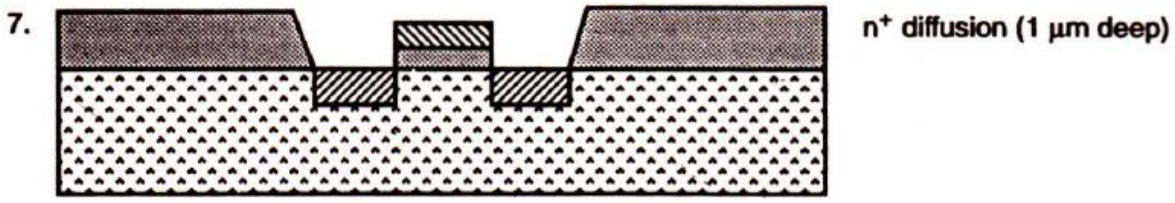
The photoresist layer is then exposed to ultraviolet light through a mask which defines those regions into which diffusion is to take place together with transistor channels.



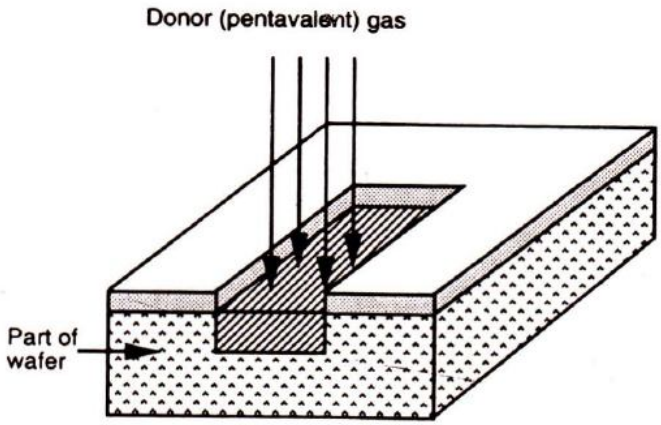
These areas are subsequently readily etched away together with the underlying silicon dioxide so that the wafer surface is exposed in the window defined by the mask.



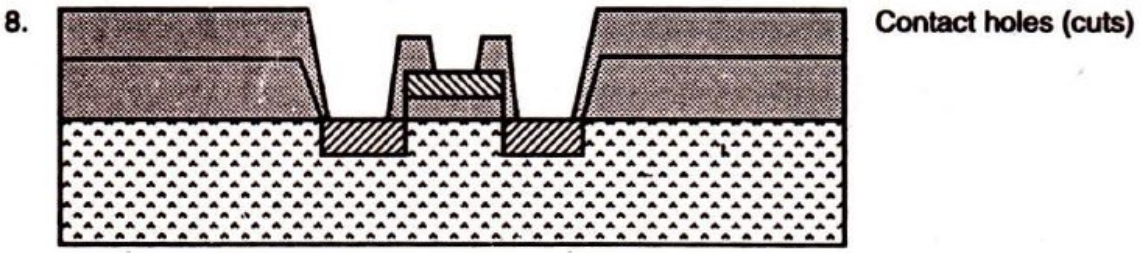
The remaining photoresist is removed and a thin layer of Si02 (0.1 jlm typical) is grown over the entire chip surface and then polysilicon is deposited on top of this to form the gate structure. Further photoresist coating and masking allows the polysilicon to be patterned.



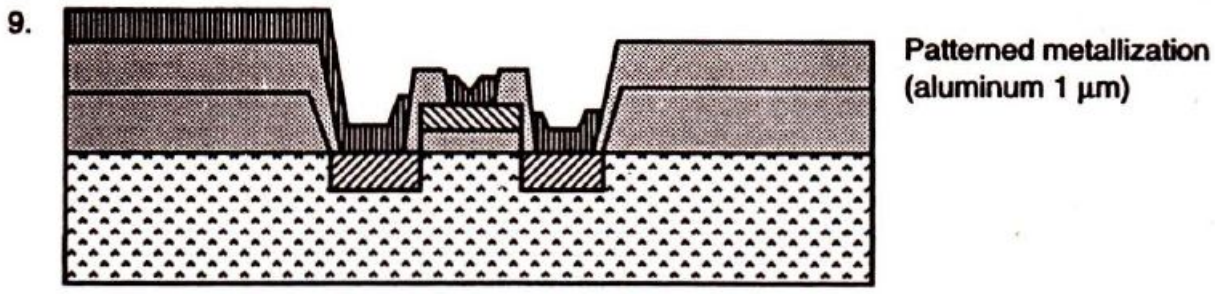
Then the thin oxide is removed to expose areas into which n-type impurities are to be diffused to form the source and drain as shown.



Diffusion is achieved by heating the wafer to a high temperature and passing a gas containing the desired n-type impurity (phosphorus) over the surface as indicated in the figure shown above.



Thick oxide (Si02) is grown over all again and is then masked with photoresist and etched to expose selected areas of the polysilicon gate and the drain and source areas where connections are to be made.

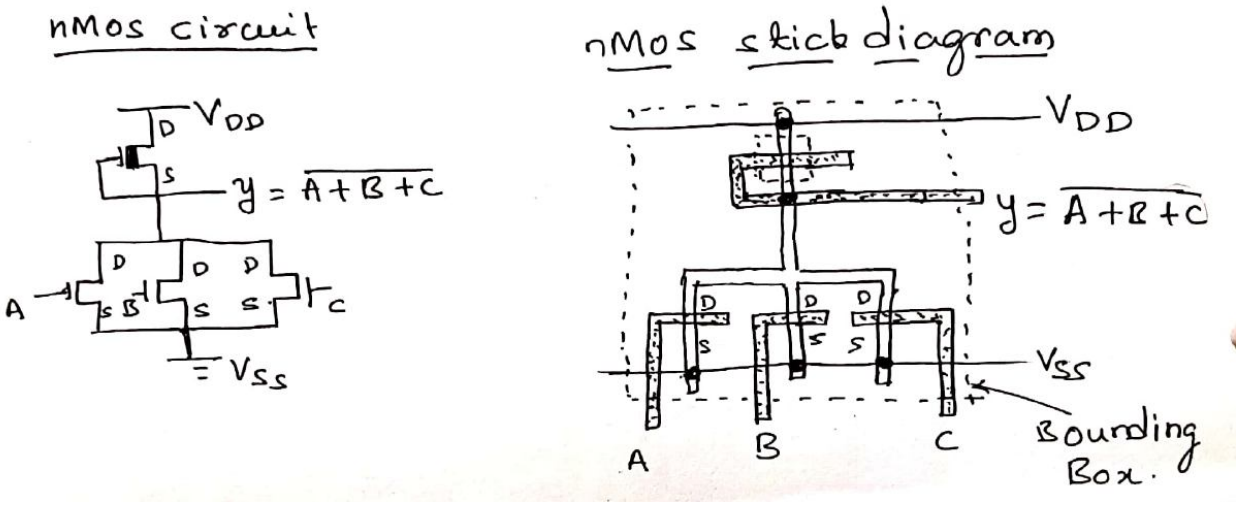


The whole chip then has metal (aluminum) deposited over its surface to a thickness typically of 1μm. This metal layer is then masked and etched to form the required interconnection pattern.

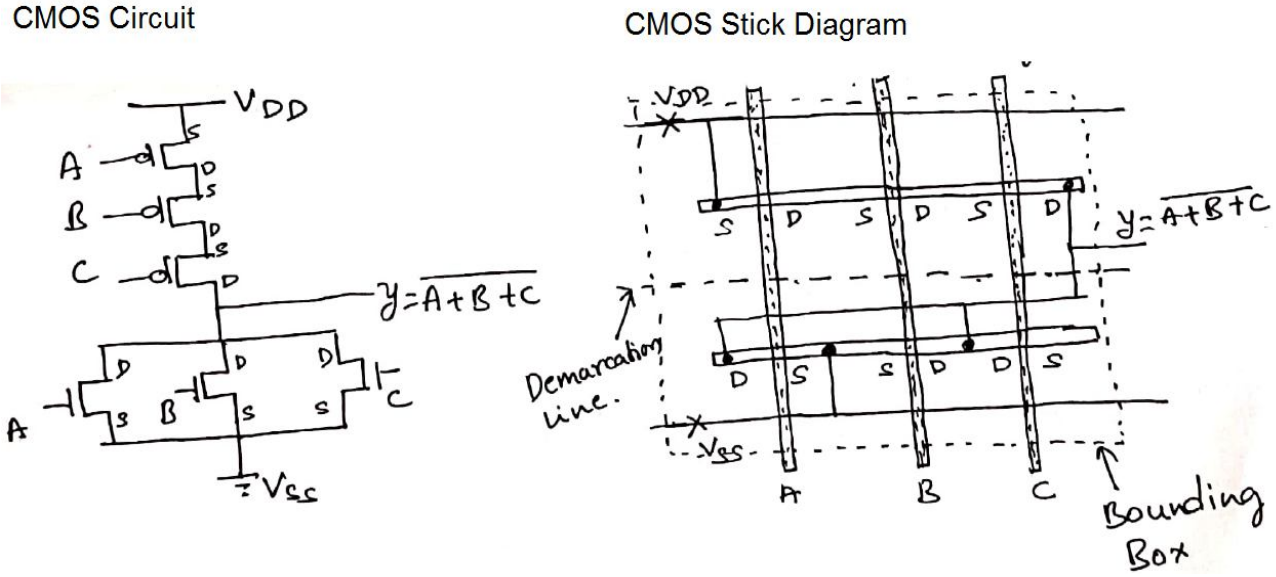
6 Marks(Diagrams) + 4 Marks(Explaination)

3 Draw the Stick Diagram for the following using nMOS and CMOS Logic:
a) $y = \overline{A + B + C}$, b) 2 input NAND Gate

a) $y = \overline{A + B + C}$



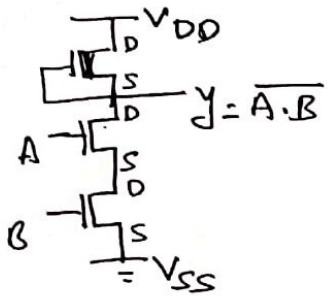
2 marks



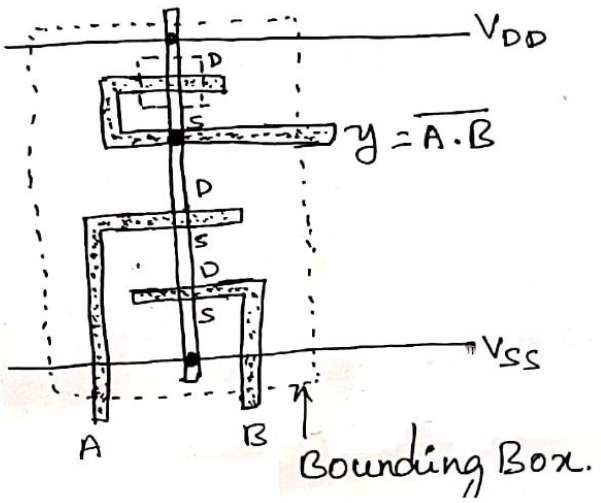
3Marks

b) 2 input NAND Gate

nMOS Circuit

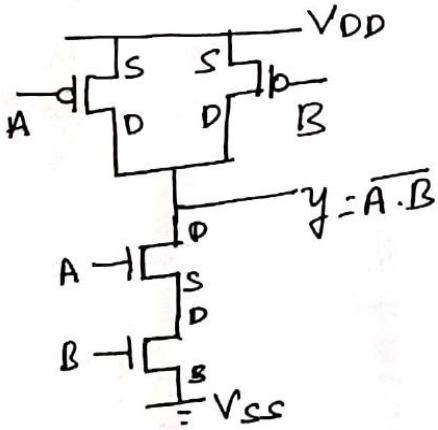


nMOS Stick Diagram

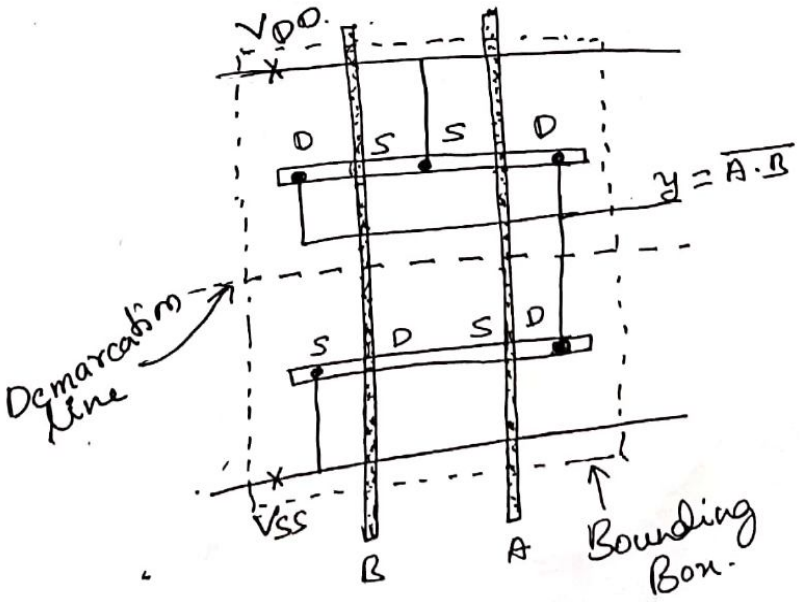


2 Marks

CMOS Circuit



CMOS Stick Diagram

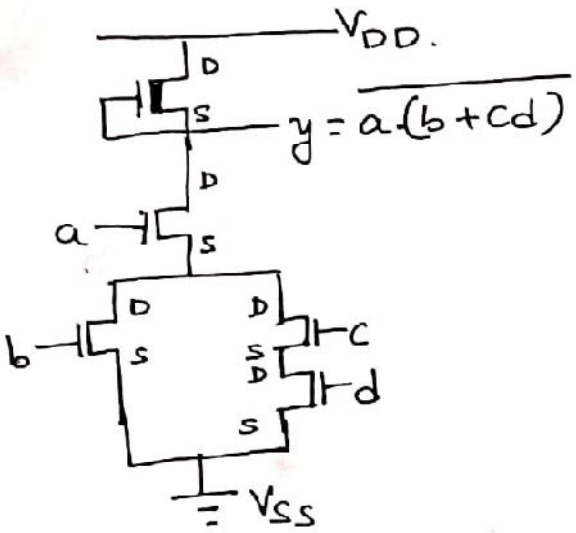


3 Marks

4 Realize the boolean expression $y = \overline{a(b + cd)}$ using nMOS and CMOS technology. Also draw the stick and layout diagram of the same in nMOS technology.

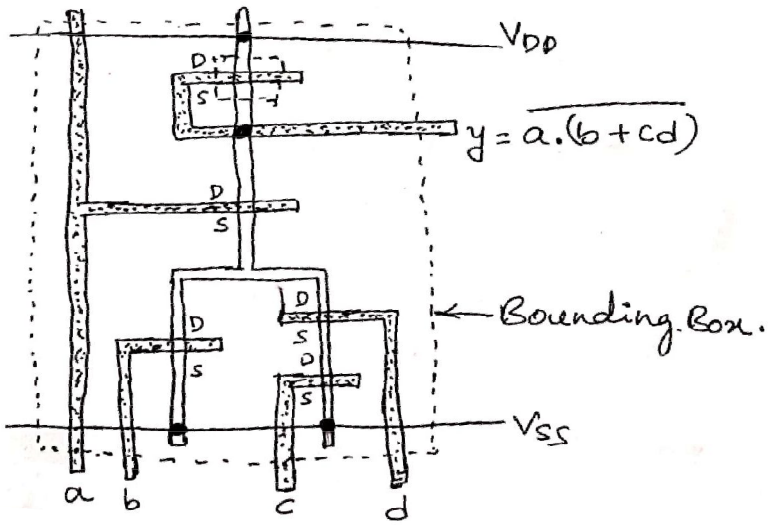
$$y = \overline{a.(b + cd)}$$

nMOS circuit



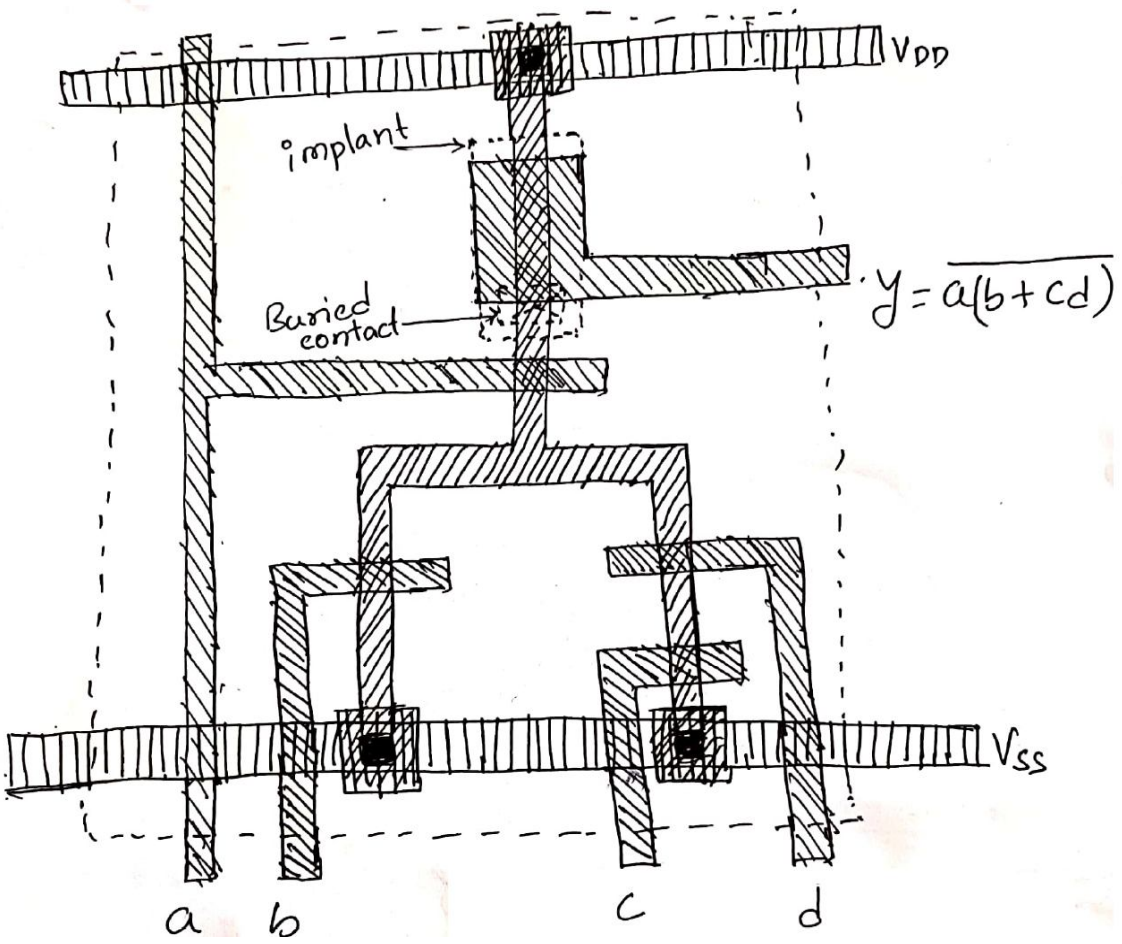
2 Marks

nMOS stick diagram



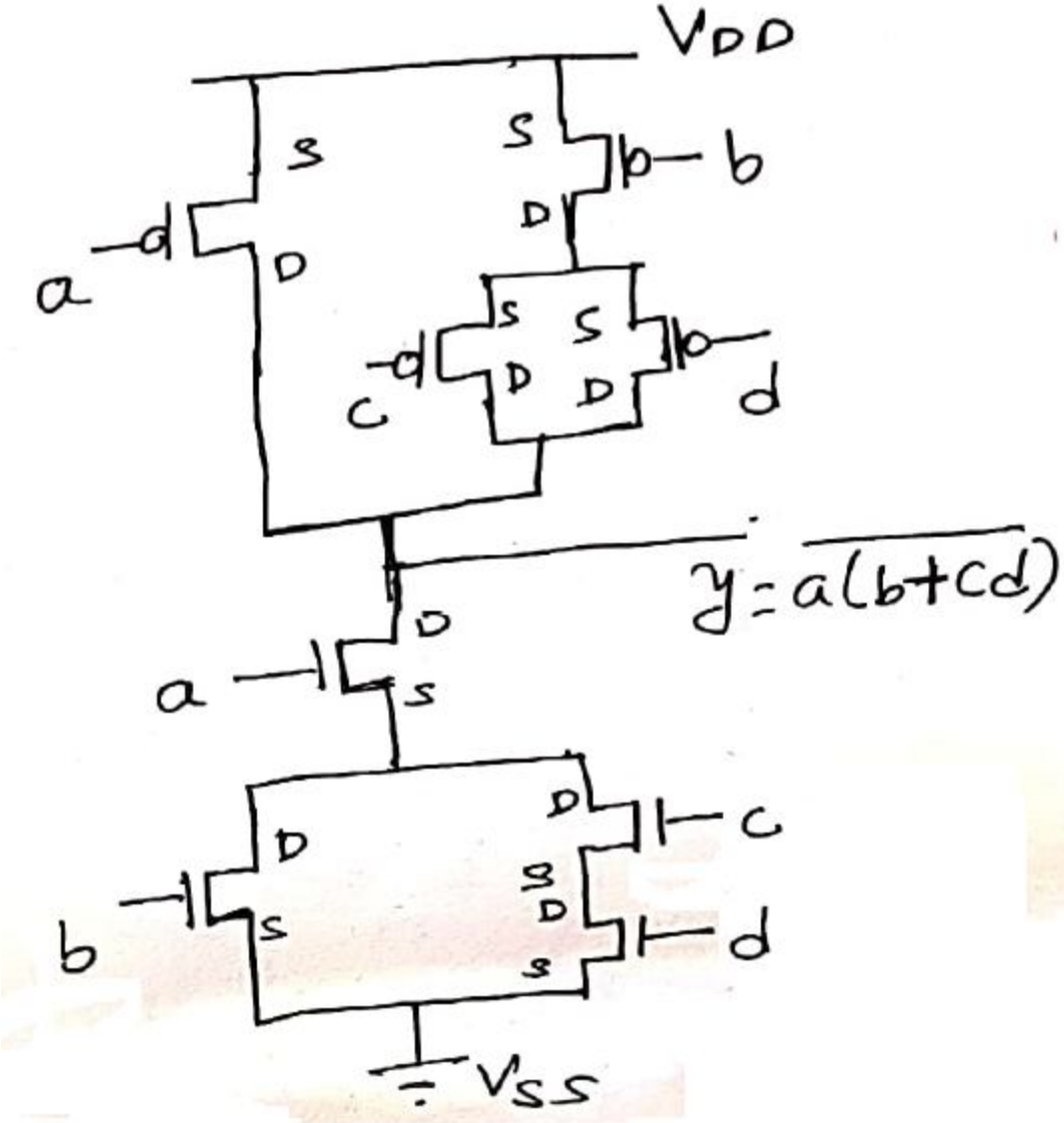
2 Marks

nMOS Mask Layout

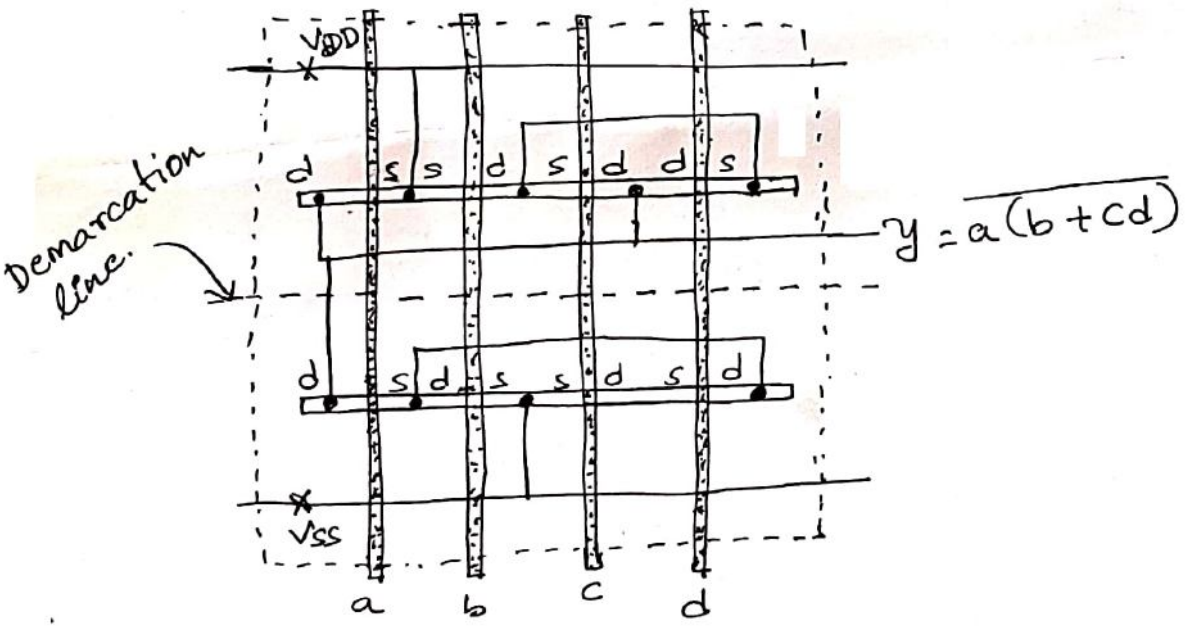


4 Marks

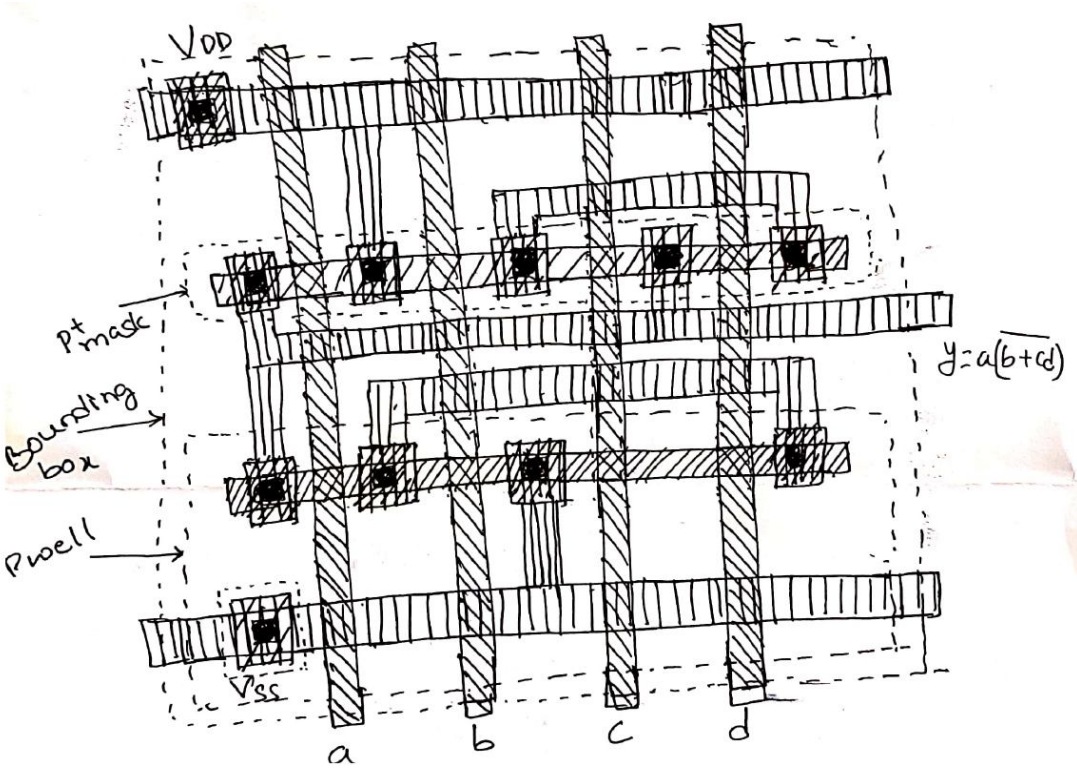
CMOS circuit



2 Marks



CMOS Stick diagram

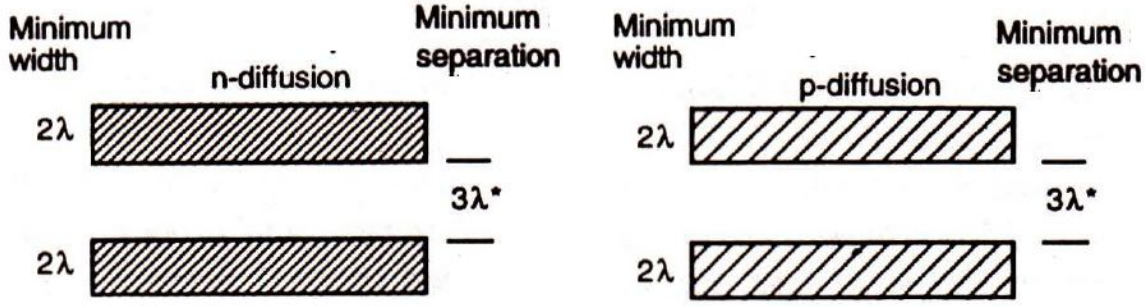


CMOS Mask Layout

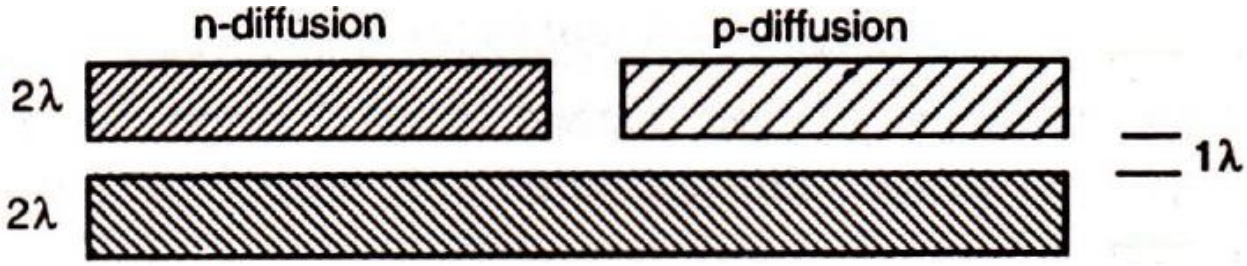
5 What are λ-based design rules? List and explain the λ-based design rules for wires and transistors.

The design rules are based on a single parameter λ which leads to a simple set of rules for the designer, and wide acceptance of the rules by a large cross-section of the fabrication houses and silicon brokers, and allows for scaling of the designs to a limited extent. Design rules and layout methodology based on the concept of A provide a process and feature size-independent way of setting out mask dimensions to scale.

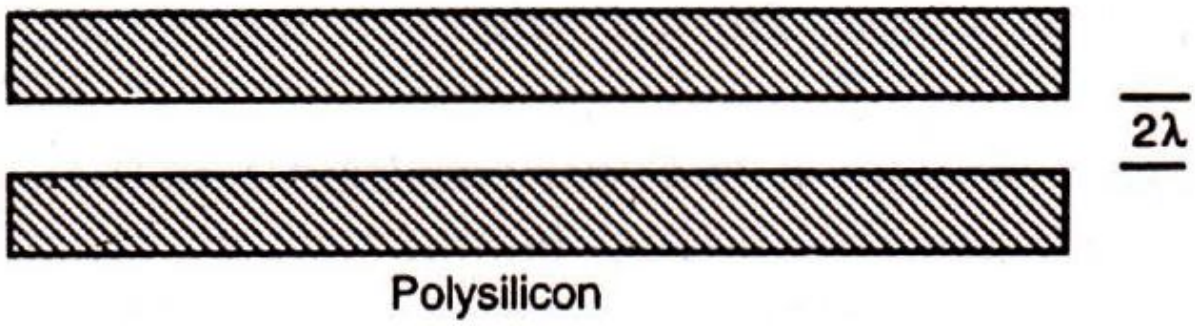
Design rules for wires



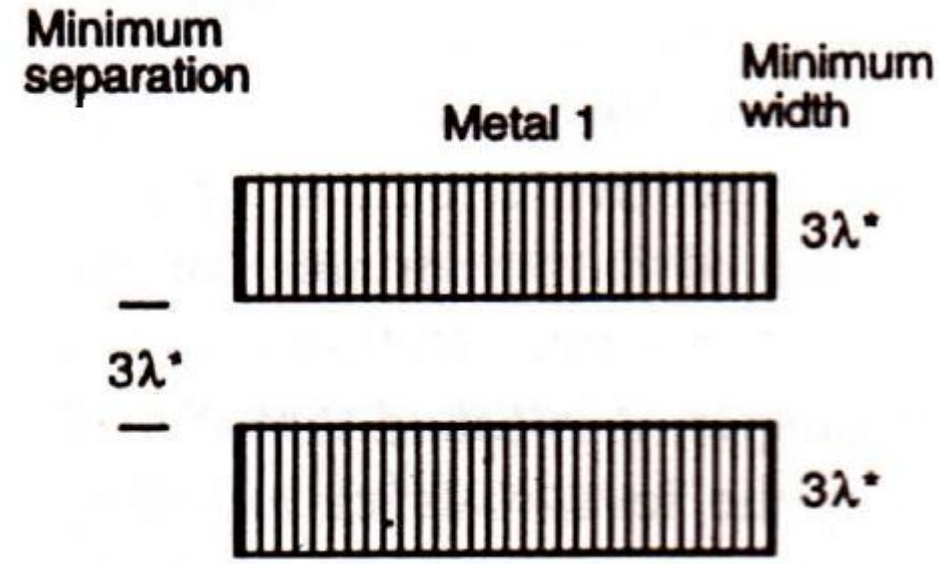
1. Minimum width of n-type or p-type diffusion wire is 2λ.
2. Minimum separation between two n-type or p-type diffusion wires is 3λ.



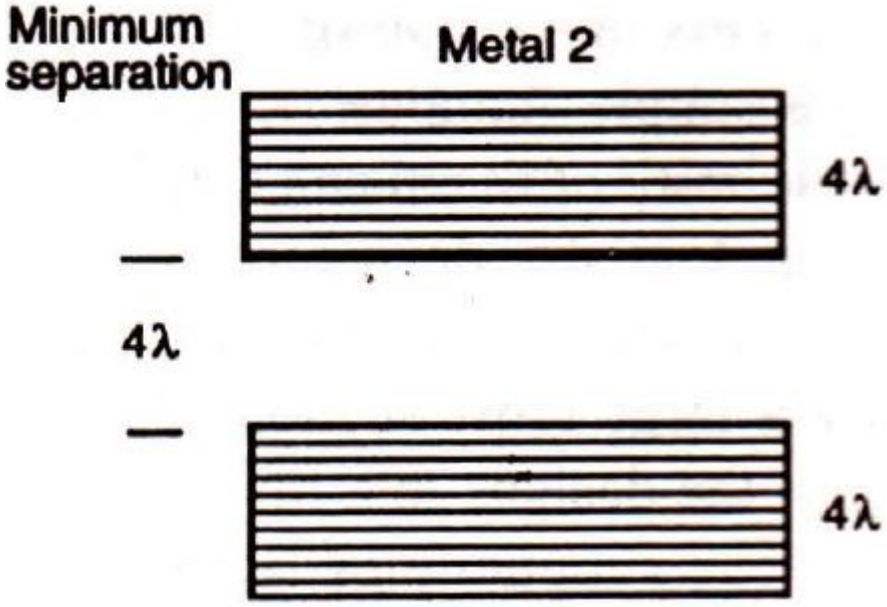
3. Minimum width of polysilicon wires is 3λ.
4. Minimum separation between any type of diffusion and polysilicon wires is is 3λ.



5. Minimum separation between two polysilicon wires is 3λ.



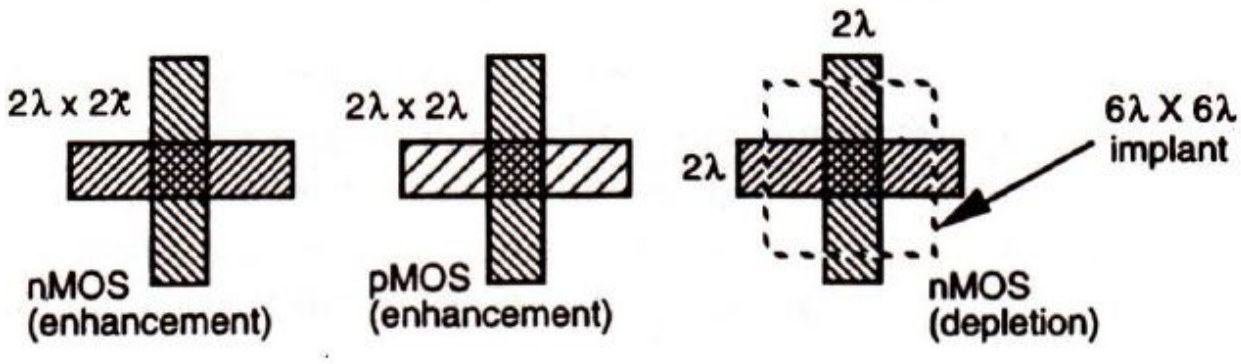
6. Minimum width of Metal 1 Layer should be 3λ.
7. Minimum separation between two Metal 1 wires is is 3λ.



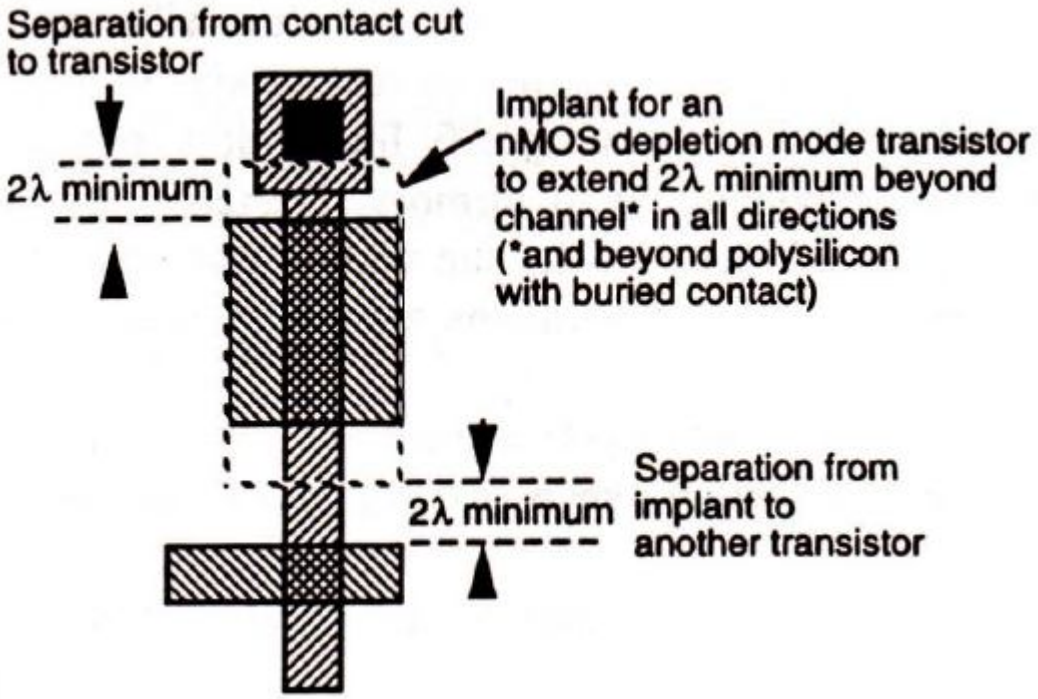
8. Minimum width of Metal 2 Layer should be 4λ.
9. Minimum separation between two Metal 2 wires is 4λ.

5 Marks

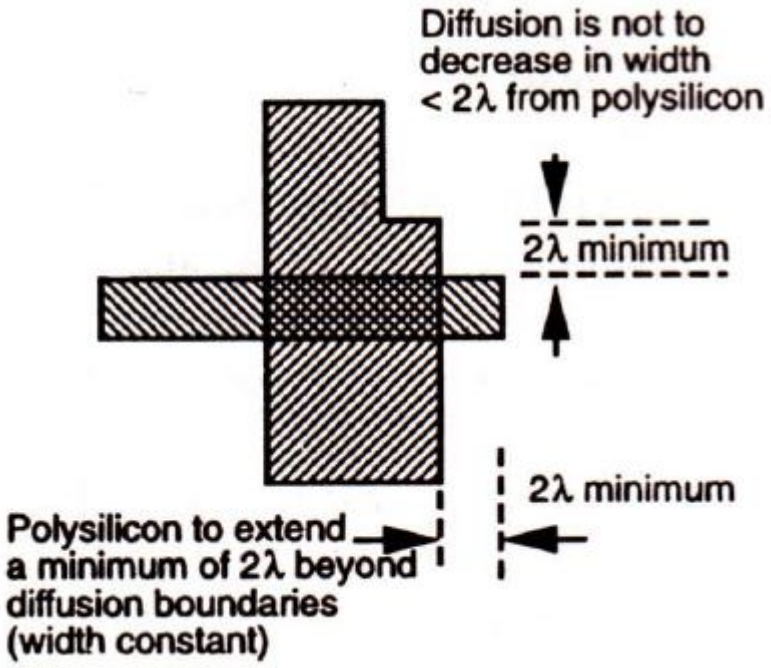
Design rules for Transistor



1. Minimum size of transistor (nMOS and pMOS) is 2λ x 2λ (Since minimum width of polysilicon and any type of diffusion is 2λ).
2. Implant layer of size 6λ x 6λ should be used for depletion mode devices around the polysilicon and diffustion crossover.



3. Minimum Separation from contact cut to transistor is 2λ.
4. Minimum Separation from implant to another transistor is 2λ.
5. Implant for an nMOS depletion mode transistor to extend 2λ minimum beyond channel in all directions



6. Minimum extension of polisilicon beyond diffusion is 2λ.
7. Minimum extension of diffusion beyond polysilicon or channel is 2λ.

5 Marks

6. Derive the expression to calculate total delay of cascaded inverters while driving the large capacitive load. [10]

4.8 DRIVING LARGE CAPACITIVE LOADS

The problem of driving comparatively large capacitive loads arises when signals must be propagated from the chip to off chip destinations. Generally, typical off chip capacitances may be several orders higher than on chip $\square C_g$ values. For example, if the off chip load is denoted C_L then

$$C_L \geq 10^4 \square C_g \text{ (typically)}$$

Clearly capacitances of this order must be driven through low resistances, otherwise excessively long delays will occur.

4.8.1 Cascaded Inverters as Drivers

Inverters intended to drive large capacitive loads must therefore present low pull-up and pull-down resistance.

Obviously, for MOS circuits, low resistance values for $Z_{p.d.}$ and $Z_{p.u.}$ imply low $L{:}W$ ratios; in other words, channels must be made very wide to reduce resistance value and, in consequence, an inverter to meet this need occupies a large area. Moreover, because of the large $L{:}W$ ratio and since length L cannot be reduced below the minimum feature size, the gate region area $L \times W$ becomes significant and a comparatively large capacitance is presented at the input, which in turn slows down the rates of change of voltage which can take place at the input.

The remedy is to use N cascaded inverters, each one of which is larger than the preceding stage by a width factor f as shown in Figure 4.11 (showing nMOS inverters, for example).

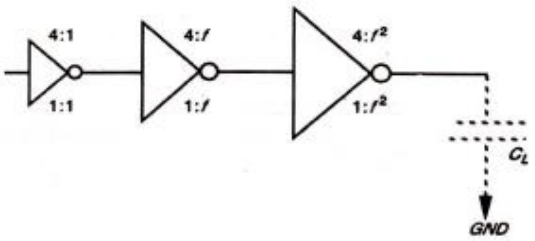


FIGURE 4.11 Driving large capacitive loads.

Clearly, as the width factor increases, so the capacitive load presented at the inverter input increases, and the area occupied increases also. Equally clearly, the rate at which the width increases (that is, the value of f) will influence the number N of stages which must be cascaded to drive a particular value of C_L. Thus, an optimum solution must be sought as follows (this treatment is attributed to Mead and Conway).

With large f, N decreases but delay per stage increases. For 4:1 nMOS inverters

delay per stage = ft for ΔV_{in}
or = $4ft$ for ∇V_{in}

where ΔV_{in} indicates logic 0 to 1 transition and ∇V_{in} indicates logic 1 to 0 transition of V_{in}

Therefore, total delay per nMOS pair = $5ft$. A similar treatment yields delay per CMOS pair = $7ft$. Now let

$$y = \frac{C_L}{\square C_g} = f^N$$

so that the choice of f and N are interdependent.

We now need to determine the value of f which will minimize the overall delay for a given value of y and from the definition of y

$$\ln(y) = N \ln(f)$$

That is

$$N = \frac{\ln(y)}{\ln(f)}$$

Thus, for N even

$$\text{total delay} = \frac{N}{2} 5ft = 2.5\ Nft \text{ (nMOS)}$$

$$\text{or} = \frac{N}{2} 7ft = 3.5\ Nft \text{ (CMOS)}$$

Thus, in all cases

$$\text{delay} \propto Nf\tau = \frac{\ln(y)}{\ln(f)} f\tau$$

It can be shown that total delay is minimized if f assumes the value e (base of natural logarithms); that is, each stage should be approximately 2.7* times wider than its predecessor. This applies to CMOS as well as nMOS inverters.

Thus, assuming that $f = e$, we have

$$\text{Number of stages } N = \ln(y)$$

and overall delay t_d

$$N \text{ even: } t_d = 2.5eN\ \tau \text{ (nMOS)}$$

$$\text{or } t_d = 3.5eN\ \tau \text{ (CMOS)}$$

$$\left.\begin{array}{l} N \text{ odd: } t_d = [2.5(N-1) + 1]e\tau \text{ (nMOS)} \\ \text{or } t_d = [3.5(N-1) + 2]e\tau \text{ (CMOS)} \end{array}\right\} \text{ for } \Delta V_{in}$$

or

$$\left.\begin{array}{l} t_d = [2.5(N-1) + 4]e\tau \text{ (nMOS)} \\ \text{or } t_d = [3.5(N-1) + 5]e\tau \text{ (CMOS)} \end{array}\right\} \text{ for } \nabla V_{in}$$

7. Obtain the scaling factors for the following parameters
i) Maximum operating frequency, ii) Channel resistance, iii) Gate capacitance per unit area, iv) Switching energy, v) Gate area [10]

i)

* Maximum Operating Frequency f_o.

$$f_o = \frac{W}{L} \frac{\mu C_o V_{DD}}{C_g}$$

or f_o is inversely proportional to delay T_d

$\therefore$ f_o is scaled by $\frac{1}{(\beta/\alpha^2)} = \frac{\alpha^2}{\beta}$.

ii)

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* Channel Resistance R_{ON}

$$R_{ON} = \frac{L}{W}\frac{1}{Q_{ON}\mu}$$

$\mu \rightarrow$ carrier mobility in the channel & is assumed constant.

$\therefore$ R_{ON} is scaled by $\left(\frac{1}{\alpha}\right)\cdot\frac{1}{(1/\alpha)}\cdot 1 = 1$

iii)

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* Gate Capacitance per unit Area C_0 or C_{ox}

$$C_0 = \frac{\epsilon_{ox}}{D}$$

ϵ_{ox} = permittivity of gate oxide (thinox)

$= \epsilon_{ins}\epsilon_0$

D = gate oxide thickness which is scaled by $(1/\beta)$.

Thus, C_0 is scaled by $\frac{1}{1/\beta} = \beta$

iv)

PROF. SUCHISMITA SENGUPTA

* Switching Energy per gate E_g –

$$E_g = \frac{1}{2}C_g (V_{DD})^2$$

$\Rightarrow$ E_g is scaled by $\left(\frac{\beta}{\alpha^2}\right)\cdot\frac{1}{\beta^2} = \left(\frac{1}{\alpha^2\beta}\right)$.

v)

* Gate Area, A_g –

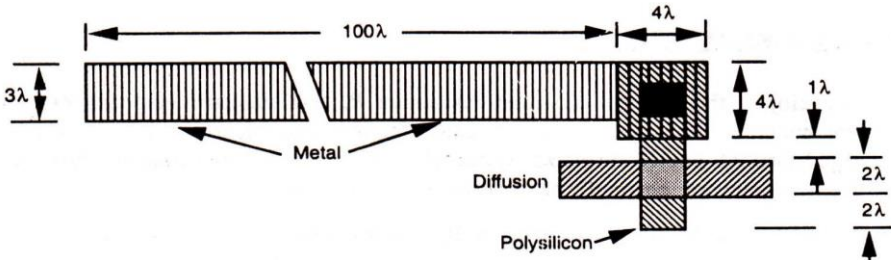
$A_g = L.W.$

L = Channel Length ; W = Channel Width

Both are scaled by $(1/\alpha)$

Thus, A_g is scaled by $(1/\alpha^2)$.

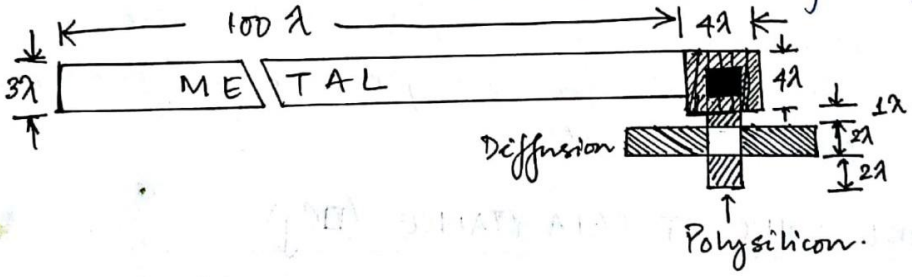
8. Calculate the area capacitance of the following structure in terms of standard unit of capacitance



(□Cg) for 5 μm process

Given: Relative capacitance of Metal1 to substrate: 0.075; Polysilicon to substrate: 0.1; Gate to channel capacitance: 1 [10]

Area of standard (feature size square) gate
$= 2\lambda \times 2\lambda$ (for λ-based rules)



Consider Metal area (less the contact region where the metal is connected to polysilicon and shielded from the substrate as the contact cut or the via is made up of Polysilicon)

$$\text{Ratio} = \frac{\text{Metal Area}}{\text{Standard gate area}} = \frac{100\lambda \times 3\lambda}{4\lambda^2} = 75$$

PROF. SUCHISMITA SENGUPTA.

Metal Capacitance, $C_M = 75 \times 0.075 = 5.625$ □Cg.

(where 0.075□Cg is the relative value for Metal1 to substrate capacitance).

Consider the Polysilicon area

Polysilicon area $= (4\lambda \times 4\lambda) + (3\lambda \times 2\lambda)$

$= 22\lambda^2$

Therefore, Polysilicon Capacitance, $C_p = \frac{22}{4} \times 0.1$

$= 0.55 \square C_g$

For the transistor, Gate Capacitance, $C_g = 1 \square C_g$.

$\Rightarrow$ Total Capacitance, $C_T = C_M + C_p + C_g$

$\approx 7.20 \square C_g$.

$\square C_g = 0.01$ pF for 5μm process.

$\therefore C_T = 72$ fF