

Internal Assesment Test - II

*******All the Best******

Solution for IAT-II

Q.1

Example $12-1$
Using a 741 op-amp, design the first-order designative low-pass filter in Fig. 12-5 to have a 1.2 kHz cutoff frequency.

Solution

From Eq. 3-1

Figure 12-5 First-order active low-pass filter circuit for Example 12-1.

$$
R_1 \approx \frac{70 \text{ mV}}{I_{\text{B(max)}}} = \frac{70 \text{ mV}}{500 \text{ nA}}
$$

$$
= 140 \text{ k}\Omega \quad \text{(use 120 k}\Omega)
$$

$$
R_2 \approx R_1 = 120 \text{ k}\Omega
$$

From Eq. 12-1

$$
C_1 = \frac{1}{2\pi R_1 f_C} = \frac{1}{2\pi \times 120 \text{ k}\Omega \times 1.2 \text{ kHz}}
$$

= 1105 pF (use 1100 pF standard value)

Second order low pass butterworth filter:

The frequency response of the 741 op-amp extends to almost 800 kHz for unity gain (see Fig. 5-9). The 741 should be suitable. Select

 $C_1 = 1000 \text{ pF}$

From Eq. 12-5

$$
R_2 = \frac{1}{2\pi f_C C_1 \sqrt{2}} = \frac{1}{2\pi \times 12 \text{ kHz} \times 1000 \text{ pF} \times \sqrt{2}}
$$

= 9.38 k\Omega (use 4.7 k\Omega + 4.7 k\Omega)
R₁ = R₂ = 9.4 k\Omega
C₂ = 2 C₁ = 2000 pF
R₃ = R₁ + R₂ = 18.8 k\Omega (use 18 k\Omega standard value)

From Eq. 12-5

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$$
f_{\rm C} = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}
$$

=
$$
\frac{1}{2\pi\sqrt{9.4 \text{ k}\Omega \times 9.4 \text{ k}\Omega \times 1000 \text{ pF} \times 2000 \text{ pF}}}
$$

= 11.97 kHz

 $Q₂$

The narrow band-reject filter, often called the notch filter, is commonly used for the rejection of a single frequency such as 60-Hz power line frequency hum. The most commonly used notch filter is the *twin-T* network shown in Figure $7-15$ (a). This is a passive filter composed of two T-shaped networks. One T network is made up of two resistors and a capacitor, while the other uses two capacitors and a resistor. The notch-out frequency is the frequency at which maximum attenuation occurs; it is given by

Unfortunately, the passive twin-T network has a relatively low figure of merit Q . The Q of the network can be increased significantly if it is used with the voltage follower as shown in Figure $7-15(b)$. The frequency response of the active notch filter of Figure $7-15(b)$ is shown in Figure $7-15(c)$. The most common use of notch filters is in communications and biomedical instruments for eliminating undesired frequencies. To design an active notch filter for a specific notch-out frequency f_N , choose the value of $C \leq 1 \mu$ F and then calculate the required value of R from Equation (7-16). For the best response, the circuit components should be very close to their indicated values.

 $Q.3$

Follow the preceding design steps.

- 1. $f_H = 1$ kHz.
- 2. Let $C = 0.01 \mu F$.
- nte e condito de la 3. Then $R = 1/(2\pi)(10^3)(10^{-8}) = 15.9 \text{ k}\Omega$. (Use a 20-k Ω potentiometer.) 4. Since the passband gain is 2, R_1 and R_F must be equal. Therefore, let $R_1 = R_F = 10 \text{ kN}$. The same is 2, R_1 and R_F must be equal. Therefore, let R_1 $R_F = 10 \text{ k}\Omega$. The complete circuit with component values is shown in Figure 7-2(a).

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- (a) A low-pass filter with $f_H = 1$ kHz was designed in Example 7-1; therefore, the same values of resistors and capacitors can be used here, that is, $R' = 15.9 \text{ k}\Omega$ and $C' = 0.01 \mu\text{F}$. As in the case of the high-pass filter, it can be designed by following the steps of section $7-3-1$:
	- 1. $f_L = 200$ Hz. 2. Let $C = 0.05 \mu F$. 3. Then

$$
R = \frac{1}{2\pi f_L C} = \frac{1}{(2\pi)(200)(5)(10^{-8})}
$$

= 15.9 kΩ

$$
f_C = \sqrt{(1000)(200)} = 447.2 \text{ Hz}
$$

$$
Q=\frac{447.2}{100-200}=0.56
$$

Thus Q is less than 10, as expected for the wide band-pass filter. $Q.A$

Ripple Rejection

The ripple rejection is a measure of how much a voltage regulator attenuates the supply voltage ripple from the unregulated power supply. It is usually $\frac{e^{i\theta}}{e^{i\theta}}$ in decibels. With a supply ripple of V_{rs} and an output ripple of V_{ro} **MOTALIJOSE SDATIOV 231852 GMA-RO SET**

$$
R_{\text{in}} \text{Pple rejection} = 20 \log \left(\frac{V_{\text{B}}}{V_{\text{m}}} \right) \tag{13-5}
$$

Source Effect

The ac supply to the input of a transformer in a dc power supply does not always remain constant. A ±10% variation in the ac source voltage is not unusual, and this causes some variation in the dc output voltage from a regulated power supply. This output voltage change (ΔV_0) due to a supply voltage change is termed the source effect. If the output varies by 100 mV when the source voltage changes by $\pm 10\%$, the source effect is 100 mV. An alternative way of stating this output change is to express ΔV_0 as a percentage of the dc output voltage (V_o) . In this case, the term line regulation is used.

Source effect =
$$
\Delta V_0
$$
 for a 10% change in supply (13-1)

Line regulation =
$$
\frac{(\Delta V_0 \text{ for a } 10\% \text{ change in } V_S) \times 100\%}{V}
$$
 (13-2)

Load Effect

Power supply output voltage is also affected by changes in load current (I_1) . The output voltage decreases when I_L is increased and rises when I_L is reduced. The load effect defines how the output voltage changes when the load current is increased from zero to its specified maximum level $(I_{L(max)})$. If the lead current change (ΔI_L) produces a voltage change (ΔV_o) of 100 mV, the load effect is 100 mV. As for the source effect, the load effect can also be expressed as a percentage of the output voltage. This is termed the load regulation.

$$
Load effect = \Delta V_o for \Delta I_{L(max)} \tag{13-3}
$$

$$
Load regulation = \frac{(\Delta V_0 \text{ for } \Delta I_{L(max)}) \times 100\%}{V_0}
$$
 (13-4)

load effect = ΔV_0 for $\Delta I_{L(max)}$ = 20 V – 19.7 V $= 300 \text{ mV}$

From Eq. 13-4

load regulation =
$$
\frac{(\Delta V_o \text{ for } \Delta I_{\text{L(max)}}) \times 100\%}{V_o}
$$

$$
= \frac{300 \text{ mV} \times 100\%}{20 \text{ V}}
$$

$$
= 1.5\%
$$

From Eq. 13-1

source effect =
$$
\Delta V_o
$$
 for a 10% change in supply = 20.2 V - 20 V
= 200 mV

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From Eq. 13-2
\nline regulation =
$$
\frac{(\Delta V_0 \text{ for a 10\% change in } V_S) \times 100\%}{V_0}
$$
\n
$$
= \frac{200 \text{ mV} \times 100\%}{20 \text{ V}}
$$
\n
$$
= 1\%
$$

For the LM317, $I_{ADJ} = 100 \mu A$ maximum. If we use $R_1 = 240 \Omega$, then for V_o of 5 V the value of R_2 from Equation (9–17b) is

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$$
(\text{normalness})_{\text{reduced}} \text{ is a constant, } \frac{1}{5} = 1.25 \left(1 + \frac{R_2}{240}\right) + (10^{-4})R_2
$$

 \pm odi os tasmislomos e ai acuatuent sunto -3.75 ^{ani} gatiov other odi in sidaliava one $R_2 = \frac{3.75}{(5.3)(10^{-3})}$ $= 0.71 \text{ k}\Omega$

Similarly, for $V_o = 12$ V, the value of R_2 is

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FIGURE 9-48 Adjustable voltage regulator for Example 9-11.

 $Q.5$

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8-3 ZERO-CROSSING DETECTOR

An immediate application of the comparator is the zero-crossing detector or sine wave-to-square wave converter. The basic comparator of Figure 8-1(a) or Figure $8-2(a)$ can be used as the zero-crossing detector provided that V_{ref} is set to zero ($V_{ref} = 0$ V). Figure 8–3(a) shows the inverting comparator used as a zerocrossing detector. The output voltage v_o waveform in Figure 8–3(b) shows when and in what direction an input signal v_{in} crosses zero volts. That is, the output v_o is driven into negative saturation when the input signal v_{in} passes through zero in the positive direction. Conversely, when v_{in} passes through zero in the negative direction, the output v_o switches and saturates positively. oveform that

GURE 8-3 (a) Zero-crossing detector. (b) Its typical input and output waveforms.

8-2 BASIC COMPARATOR

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Figure 8-1(a) shows an op-amp used as a comparator. A fixed reference voltage V_{ref} of 1 V is applied to the $(-)$ input, and the other time-varying signal voltage v_{in} is applied to the (+) input. Because of this arrangement, the circuit is called the noninverting comparator. When v_{in} is less than $\widetilde{V}_{\text{ref}}$, the output voltage v_o is at $-V_{\text{sat}} \ (\cong -V_{EE})$ because the voltage at the $(-)$ input is higher than that at the (+) input. On the other hand, when v_{in} is greater than V_{ref} , the (+) input becomes positive with respect to the (-) input, the v_o goes to + V_{sat} (\cong + V_{cc}). Thus v_0 changes from one saturation level to another whenever $v_{in} \cong V_{ref}$, as shown in Figure $8-1(b)$. In short, the comparator is a type of analog-to-digital converter. At any given time the v_0 waveform shows whether v_{in} is greater or less than V_{ref} . The comparator is sometimes also called a *voltage-level detector* because, for a detector of the comparator is sometimes also called a *voltage-level detector* because, for a desired value of V_{ref} , the voltage level of the input v_{in} can be detected.

In Figure $8-4(a)$, these threshold voltages are obtained by using the voltage divider $R_1 - R_2$, where the voltage across R_1 is fed back to the (+) input. The voltage across R_1 is a variable reference threshold voltage that depends on the value and polarity of the output voltage v_o . When $v_o = +V_{\text{sat}}$, the voltage across R_1 is called the *upper threshold voltage*, V_{ut} . The input voltage v_{in} must be slightly

more positive than V_{ut} in order to cause the output v_o to switch from $+V_{sat}$ to V_{sat} . As long as $v_{\text{in}} < V_{\text{ut}}$, v_o is at $+V_{\text{sat}}$. Using the voltage-divider rule,

 $V_{\rm IR}$ P^* =

$$
V_{\rm ut} = \frac{R_1}{R_1 + R_2} \left(+ V_{\rm sat} \right) \tag{8-1a}
$$

On the other hand, when $v_o = -V_{\text{sat}}$, the voltage across R_1 is referred to as the lower threshold voltage, V_{lt} , v_{in} must be slightly more negative than V_{lt} in order to cause v_o to switch from $-V_{\text{sat}}$ to $+V_{\text{sat}}$. In other words, for v_{in} values greater than V_{1t} , v_o is at $-V_{sat}$. V_{1t} is given by the following equation:

$$
V_{1t} = \frac{R_1}{R_1 + R_2} \left(-V_{\text{sat}} \right)
$$
 (8–1b)

Thus, if the threshold voltages V_{ut} and V_{lt} are made larger than the input noise voltages, the positive feedback will eliminate the false output transitions. Also, the positive feedback, because of its regenerative action, will make v_0 switch faster between $+V_{\text{sat}}$ and $-V_{\text{sat}}$. In Figure 8–4(a), resistance $R_{OM} \cong R_1 || R_2$ is used to minimize the offset problems.

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 $F = F - F - F - F - F - H$

For 741 the maximum output voltage swing is \pm 14 V, that is, $+V_{\text{sat}} = 14$ V and $-V_{\text{sat}} = -14$ V. From Equations (8–1a) and 8–1b),

$$
\frac{1}{2} \cdots \frac{1}{2} \left(\frac{1}{2} \right)
$$

$$
V_{\text{ut}} = \frac{100}{56,100} (14) = 25 \text{ mV}
$$

and homeforman of each to operator and $V_h = \frac{100}{56,100}$ (-14) = -25 mV and meaning the set $\frac{1}{200}$ (-14) = -25 mV and meaning the set of the

The output v_o waveform is shown in Figure 8-4(b). From Equation (8-2), the hysteresis voltage $V_{\text{hy}} = 50 \text{ mV}$.