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Internal Assesment Test - III

Sub:	OPERATIONAL AMPLIFIERS & LINEAR ICS						Code:	17EE46
Date:	15/05/2019	Duration:	90 mins	Max Marks:	50	Sem:	4th(A & B)	Branch:	EEE

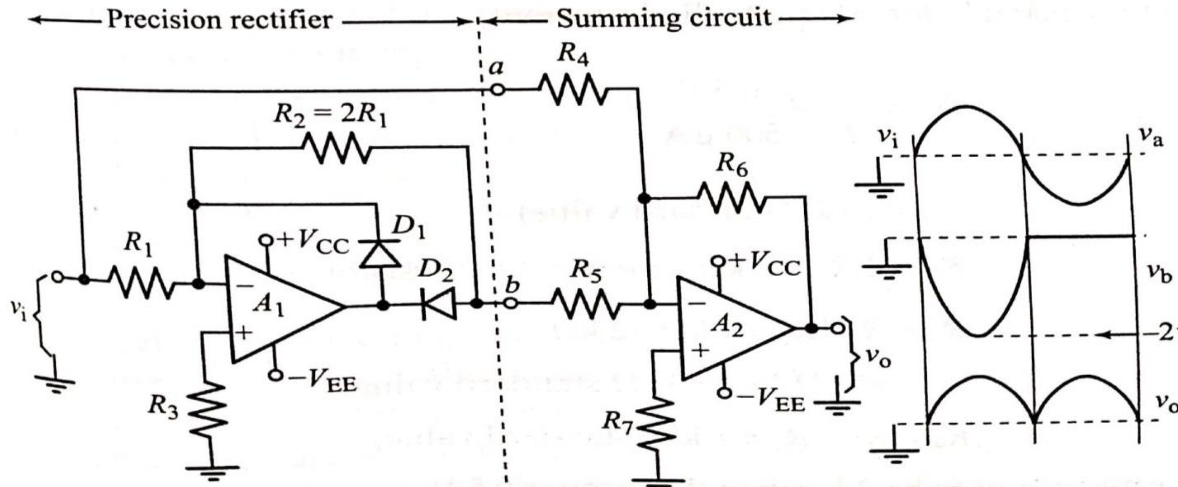
Answer any five questions.

		Marks	OBE	
			CO	RBT
1	Explain the circuit of a full wave precision rectifier using half wave rectifiers and summing circuit. Demonstrate the input and output waveforms.	10	CO3	L2
2	Explain the working of R-2R ladder DAC. In 8 bit DAC has an output voltage of 0-2.55 V. Define its resolution in two different ways.	10	CO2	L2
3	What is the major limitation of conventional rectifier? Explain the working of precision positive and negative half wave rectifier using noninverting type.	10	CO3	L3
4	Explain the operating principle of PLL. Define lock range and capture range, pull in time.	10	CO5	L2
5	Design a nonsaturating half wave rectifier to produce a 2 V peak output from a 1 MHz sine wave input with a 0.5 peak value.Use a bipolar op-amp with a supply voltage of +/- 15 V.(I_1 =500 μ A) If the R-2R DAC is expressed into a 5 bit. Calculate the analog output voltage when the input is (i)00001 (ii) 10000 (iii)11111	10	CO3	L3
6	Discuss the operation of successive approximation ADC with circuit diagram.	10	CO2	L3`
7	Explain the working of PLL with block diagram. Explain the function of each block in detail.Design a square waveform generator of frequency 100 Hz and duty cycle of 75%.	10	CO6	L2

Q.1

Half-Wave Rectifier and Summing Circuit

The left side of the circuit in Fig. 9-4 is a precision half-wave rectifier as in Fig. 9-2, but with the diodes reversed. The right side is an inverting summing amplifier circuit (explained in Section 3-6). The input voltage is applied to terminal *a* of the summing amplifier and to the input of the precision rectifier. Note that resistor R_2 in the precision half-wave rectifier circuit has twice the resistance of R_1, so the rectified voltage applied to terminal *b* of the summing amplifier is $-2v_i$, as illustrated.



During the positive half-cycle of the input, the voltage at terminal *a* is $+v_i$, while that at terminal *b* is $-2v_i$. The output from the summing circuit with $R_5 = R_4$ is

$$v_o = \frac{-R_6}{R_4}(v_a + v_b) = \frac{-R_6}{R_4}(v_i - 2v_i)$$

$$= \frac{R_6}{R_4} v_i$$

During the negative half-cycle of the input, $v_a = -v_i$ and $v_b = 0$. Consequently, the output is

$$v_o = \frac{-R_6}{R_4}(-v_i + 0)$$

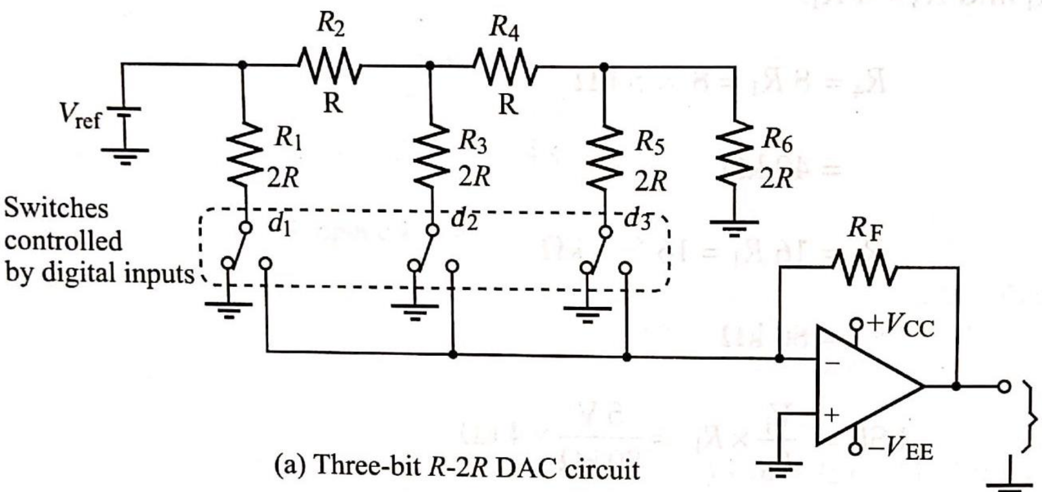
$$= \frac{R_6}{R_4} v_i$$

It is seen that the output is a full-wave rectified version of the input voltage. If resistor R_6 equals R_4 and R_5, the circuit has an overall voltage gain of 1. When R_6 is greater than R_4 and R_5, amplification and rectification both occur. A *precision full-wave rectifier* circuit is also known as an *absolute value* circuit. This means the circuit output is the absolute value of the input peak voltage regardless of the input polarity.

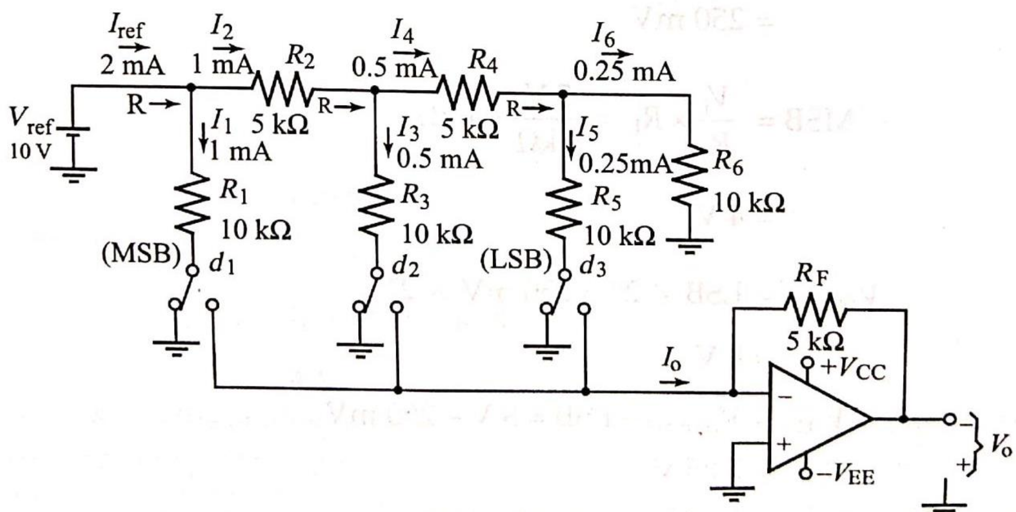
Q.2

R-2R DAC

Figure 15-6(a) shows a 3-bit DAC circuit that uses only two resistor values (R and $2R$), and so this circuit is much more suitable for IC fabrication than the weighted-resistor DAC. In addition to the resistor relationship, note that the circuit uses a reference voltage (V_{ref}) and switches that set one end of resistors R_1, R_3, and R_5 either to ground or to the op-amp inverting input terminal. This arrangement is a more accurate substitute for applying the digital bits directly as inputs (as in Fig. 15-4) because the bit amplitudes are unlikely



(a) Three-bit *R*-2*R* DAC circuit



(b) Resistance values and currents in a 3-bit *R*-2*R* DAC circuit

$$V_o = \frac{V_{ref} R_F}{R}\left(\frac{d_1}{2^1} + \frac{d_2}{2^2} + \frac{d_3}{2^3} + \frac{d_4}{2^4} + \cdots + \frac{d_n}{2^n}\right)$$

to be predictable with any degree of accuracy. The switches (usually FETs) are controlled by the digital input bits so that they are set to ground when a bit is absent or to the (virtual ground) op-amp input when the bit is present. This means that there is always a constant current through each resistor regardless of the switch position and that the resistor currents track each other with temperature changes.

Digital inputs d_1	d_2	d_3	Analog outputs	
0	0	1	0.25 mA × 5 kΩ	= 1.25 V
0	1	0	0.5 mA × 5 kΩ	= 2.5 V
0	1	1	0.75 mA × 5 kΩ	= 3.75 V
1	0	0	1 mA × 5 kΩ	= 5 V
1	0	1	1.25 mA × 5 kΩ	= 6.25 V
1	1	0	1.5 mA × 5 kΩ	= 7.5 V
1	1	1	1.75 mA × 5 kΩ	= 8.75 V

Figure 15-7 Digital inputs and the resultant analog outputs for the DAC in Fig. 15-6(b).

The R-$2R$ DAC circuit is reproduced in Fig. 15-6(b) with $R = 5\ \text{k}\Omega$ and $2R = 10\ \text{k}\Omega$ resistor values and with a 10 V reference source. Note that when looking from resistor R_4 into the junction of R_5 and R_6, the resistance seen is $R_5 \| R_6 = (2R)\|(2R) = R = 5\ \text{k}\Omega$. Looking from R_2 into the R_3-R_4 junction, the resistance is again $(2R)\|(2R) = R$. Looking from the reference source into the R_1-R_2 junction, once more the resistance is $(2R)\|(2R) = R$. So, the reference source current is

$$I_{ref} = \frac{V_{ref}}{R} = \frac{10\ \text{V}}{5\ \text{k}\Omega}$$

$$= 2\ \text{mA}$$

Moving from the R_1-R_2 junction toward R_1 and R_2, a $2R$ resistance (10 kΩ) is offered in each branch. So, I_{ref} splits up into equal 1 mA levels in R_1 and R_2. Similarly, the 1 mA current through R_2 splits into 0.5 mA in R_3 and R_4, and the 0.5 mA in R_4 splits into 0.25 mA in R_5 and R_6. Depending upon the switch positions, currents I_1, I_3, and I_5 add to give I_o, which results in $V_o = (I_o R_F)$.

The table in Fig. 15-7 shows the result of all combinations of digital bit inputs. A 001 input, for example, causes only current I_3 to be switched to the op-amp input so that I_3 flows through R_F to produce a 1.25 V analog output. This is the LSB. Similarly, when the input is 100, $I_o = I_1$, and $V_o = 5$ V, which is the MSB. When all three digital inputs are switched to the op-amp inverting terminal (a 111 digital input), $I_1 + I_3 + I_5$ flows through R_F to give an 8.75 V output. Note that the use of an inverting amplifier at the DAC output gives a negative analog output voltage. A positive output can be produced by using a negative reference voltage source.

The equation for the analog output from the 3-bit R-$2R$ DAC can be written as

$$V_o = \frac{V_{ref} R_F}{R}\left(\frac{d_1}{2} + \frac{d_2}{4} + \frac{d_3}{8}\right)$$

where d_1, d_2, and d_3 are either 1 or 0, depending upon the presence or absence of each digital input bit. The equation can be rewritten and expanded for a DAC with any number of digital input bits

Q.2

$$n = \text{Number of bits} = 8$$

i) Resolution $= 2^n = 2^8 = 256$

i.e. the output voltage can have 256 different values including zero.

ii) V_{oFS} = Full scale output voltage

$= 2.55$ V

$$\therefore \quad \text{Resolution} = \frac{V_{oFS}}{2^n - 1} = \frac{2.55}{2^8 - 1} = \frac{10 \text{ mV}}{1 \text{ LSB}}$$

Thus an input change of 1 LSB causes the output to change by 10 mV.

Q.3

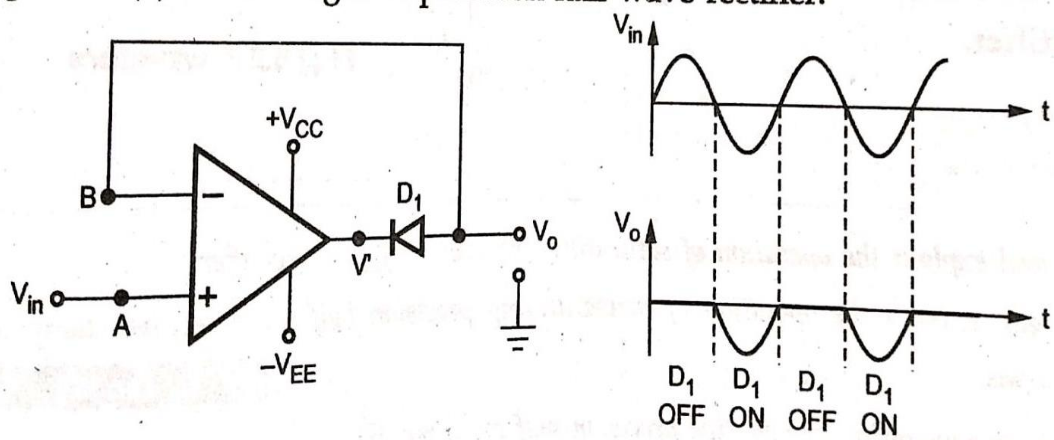
The advantages of op-amp precision rectifier circuits over simple diode rectifiers are as follows:

1. No diode voltage drop between input and output.
2. The ability to rectify very small voltages (much smaller than the typical 0.7 V diode forward voltage drop).
3. Amplification, if required.
4. Low output impedance.

Items (1) and (2) indicate that the precision rectifier is a close approximation to an ideal diode.

Negative Precision Half Wave Rectifiers

Fig. 6.2.5 (a) shows negative precision half wave rectifier.



(a) Circuit (b) Waveforms

Fig. 6.2.5 Negative precision half wave rectifier

When V_{in} is Positive, instantaneously V' goes high and diode is reverse biased acts as open circuit. Hence $V_o = 0$ V.

When V_{in} is negative, instantaneously V' goes low and diode is forward biased and acts as short circuit. The feedback path is complete and circuit acts as voltage follower. Thus $V_o = V_B = -V_{in}$ due to virtual ground. Hence output is negative half cycle of the input produced as it is. The waveforms are shown in the Fig. 6.2.5 (b).

Another type of negative precision half wave rectifier is shown in the Fig. 6.2.6. The op-amp A is in inverting mode. When V_{in} is positive, due to high open loop gain, V' is highly negative. This makes D_1 forward biased and D_2 reverse biased. Thus feedback path gets established and circuit acts as inverting amplifier.

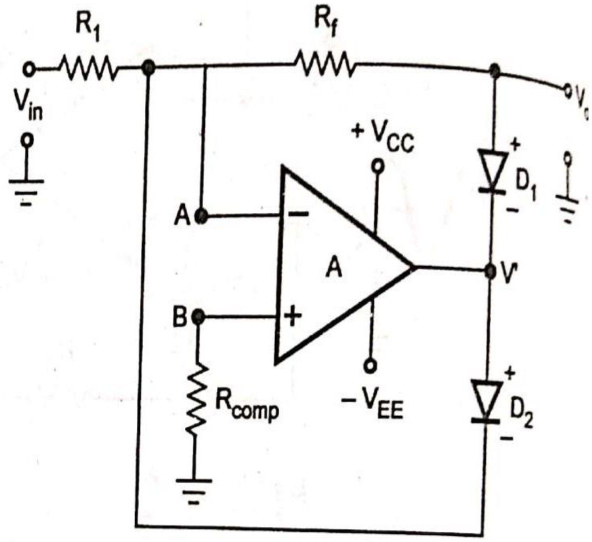


Fig. 6.2.6

$$\therefore \quad V' = -\frac{R_f}{R_1} V_{in} = V_o \qquad \text{... } D_1 \text{ acts as short circuit}$$

using $R_f = R_1$, $V_o = -V_{in}$ and output produces negative half cycle.

When V_{in} is negative, due to high A_{OL}, instantly V' becomes positive hence D_1 is reverse biased D_2 is forward biased. As D_1 is open $V_o = 0$ and diode D_2 prevents op-amp to go into saturation. The waveforms are shown in the Fig. 6.2.7.

As negative half cycle is produced for positive half cycle of input, the circuit is called the **inverting half wave precision negative rectifier.**

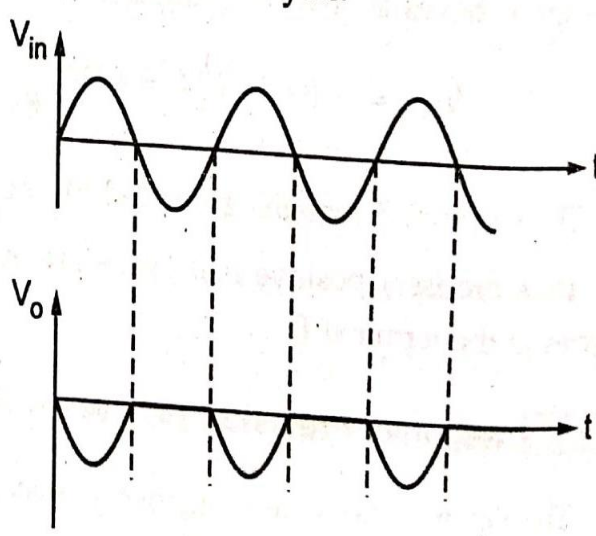


Fig. 6.2.7 wavefors

6.2.1 Saturating Precision Half Wave Rectifiers

The saturating precision half wave rectifiers circuit is obtained from voltage follower circuit by connecting a diode in between op-amp output terminal and circuit output terminal. It is shown in the Fig. 6.2.1.

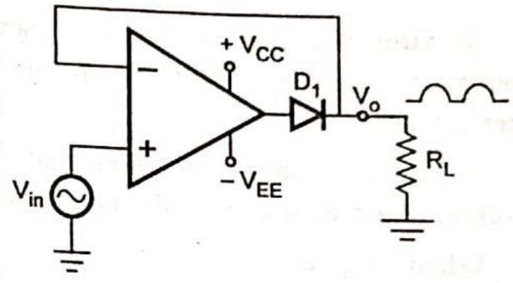


Fig. 6.2.1 Saturating precision half wave rectifier

When input V_{in} is positive going, the op-amp produces positive saturation voltage. This makes diode D_1 forward biased and circuit acts as normal voltage follower giving $V_o = V_{in}$. Due to high open loop gain, within microvolts of input, the diode conducts. The diode forward voltage is not involved in the operation hence entire positive half cycle of V_{in} is precisely available at the output. This is shown in the Fig. 6.2.2 (a).

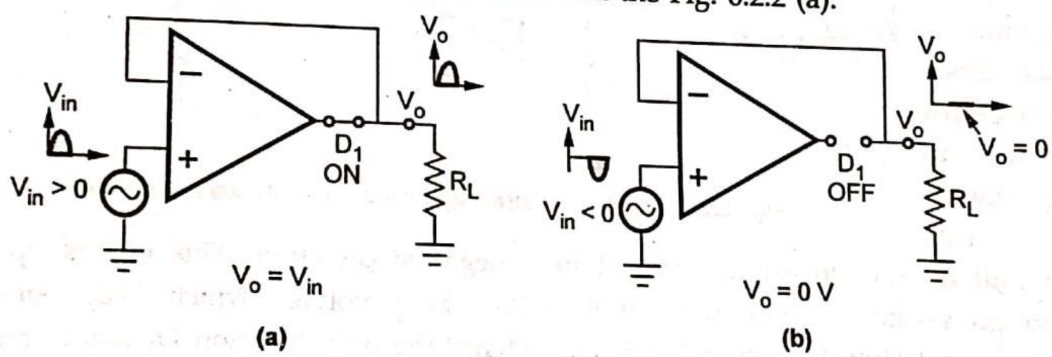


Fig. 6.2.2 Saturated precision half wave rectifier

When V_{in} goes negative, op-amp output attains negative saturation voltage and diode D_1 is reverse biased. Due to open diode, feedback path gets opened and inverting terminal remains at ground potential as R_L is grounded. Thus $V_o = 0$ and negative half cycle of V_{in} is clipped off. This is shown in the Fig. 6.2.2 (b)

For positive input cycle, the positive output cycle is produced at the output hence the circuit is called noninverting half wave precision rectifier.

The waveforms are shown in the Fig. 6.2.3.

By changing the direction of diode in this circuit, a negative half wave precision rectifier can be obtained in which positive half cycle of the input gets clipped off and negative half cycle produced at the output as it is.

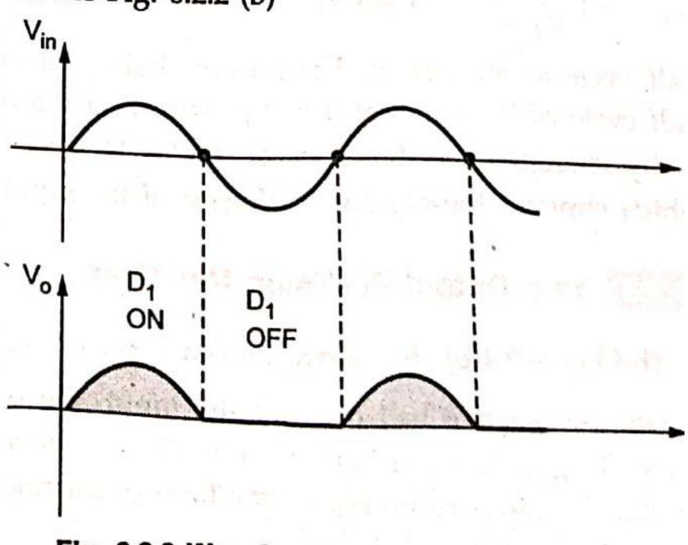


Fig. 6.2.3 Waveforms of half wave precision rectifier

Q.4

A phase-locked loop (PLL) system accepts an input voltage waveform and generates another wave that is *phase-locked* to the input. The generated wave has a frequency exactly equal to the input frequency and is normally phase-shifted from the input by a fixed phase angle. Feedback from the output prevents the frequency of the generated wave from drifting away from equality

LOCK RANGE : When PLL is in lock, it can track frequency changes in the incoming signal. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the **lock range** or **tracking range** of the PLL. It is usually expressed as a percentage of f_o, the VCO frequency.

CAPTURE RANGE : The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. It is also expressed as a percentage of f_o.

PULL-IN TIME : The capture of an input signal does not take place as soon as the signal is applied, but it takes finite time. The total time taken by the PLL to establish a lock is called **pull-in time**. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop again and the bandwidth of the lowpass filter.

Q.5

$$R_2 = \frac{v_o}{I_1} = \frac{2\text{ V}}{500\ \mu\text{A}}$$

$$= 4\text{ k}\Omega \quad (\text{use } 3.9\text{ k}\Omega \quad \text{standard value})$$

$$R_3 = R_1 || R_2 = 1\text{ k}\Omega\, || 3.9\text{ k}\Omega$$

$$= 796\ \Omega\ (\text{use } 820\text{ v standard value})$$

For diodes D_1 and D_2,

$$V_R > [V_{CC} - (-V_{EE})] > [15\text{ V} - (-15\text{ V})]$$

$$> 30\text{ V}$$

Select

$$t_{rr(max)} = 0.1\ T = \frac{0.1}{f} = \frac{0.1}{1\text{ MHz}}$$

$$= 0.1\ \mu\text{s}$$

Compensate the op-amp as a voltage follower.

Select $I_1 = 500\ \mu A$ (for adequate diode current)

$$R_1 = \frac{v_1}{I_1} = \frac{0.5\ V}{500\ \mu A}$$

$$= 1\ k\Omega \quad \text{(standard value)}$$

$$V_o = \frac{V_{ref} R_F}{R}\left(\frac{d_1}{2^1} + \frac{d_2}{2^2} + \frac{d_3}{2^3} + \frac{d_4}{2^4} + \cdots + \frac{d_n}{2^n}\right)$$

$$= \frac{10\ V \times 5\ k\Omega}{5\ k\Omega}\left(\frac{0}{2^1} + \frac{0}{2^2} + \frac{0}{2^3} + \frac{0}{2^4} + \frac{1}{2^5}\right)$$

$$= 312.5\ mV = LSB$$

(b)

$$V_o = \frac{10\ V \times 5\ k\Omega}{5\ k\Omega}\left(\frac{1}{2^1} + \frac{0}{2^2} + \frac{0}{2^3} + \frac{0}{2^4} + \frac{0}{2^5}\right)$$

$$= 5\ V\ MSB$$

(c)

$$V_o = \frac{10\ V \times 5\ k\Omega}{5\ k\Omega}\left(\frac{1}{2^1} + \frac{1}{2^2} + \frac{1}{2^3} + \frac{1}{2^4} + \frac{1}{2^5}\right)$$

$$= 9.6875\ V$$

or from Eq. 15-1

$$V_{(max)} = LSB \times 2^n = 312.5\ mV \times 2^5$$

$$= 10\ V$$

and Eq. 15-2

$$V_{(FS)} = V_{(max)} - LSB = 10\ V - 312.5\ mV$$

$$= 9.6875\ V$$

Q.6

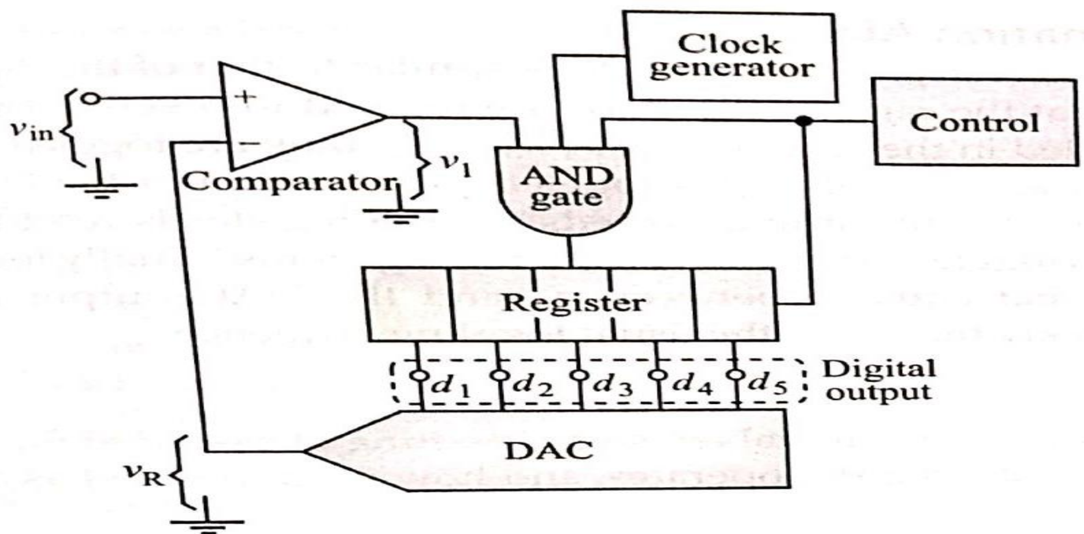
Successive Approximation ADC

The operation of a *successive approximation ADC* is similar to that of the digital ramp-type, except that the register flip-flops are toggled in reverse. That is, instead of being toggled in the sequence d_5-d_4-d_3-d_2-d_1, they are toggled in the d_1-d_2-d_3-d_4-d_5 sequence. The MSB (d_1) is toggled first, instead of the LSB (d_5). If this produces a DAC output that exceeds v_{in}, the register is reset to zero and the next MSB is toggled. The result is that the register is initially toggled in large steps so that equality between v_{in} and the DAC output is reached much more quickly than with the usual toggling sequence.

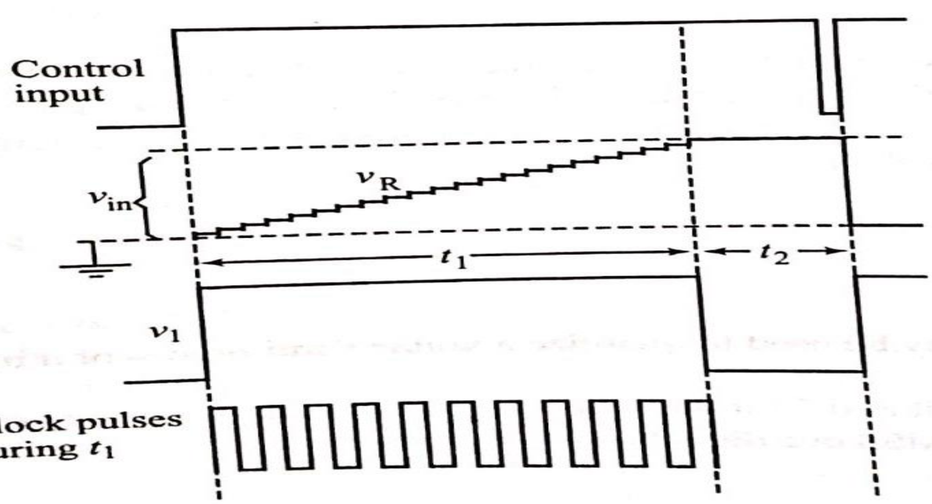
Digital Ramp ADC

The *digital ramp ADC* shown in Fig. 15-18(a) is a modified version of the linear ramp ADC discussed above. The ramp generator in Fig. 15-16 is replaced with a DAC, which converts the digital output back to analog. As illustrated in Fig. 15-18(b), the output waveform from the DAC is a *staircase*, incremented by each clock pulse passed to the register. A rectangular-wave *control* input is used to cycle the system through the conversion process. The leading edge of the control input pulse resets the register to zero at the commencement of the conversion cycle, and applies a high input to the (three-input) AND gate. At this instant, the analog input is greater than the DAC output and so the comparator output is high, thus allowing the AND gate to pass clock pulses to toggle the register.

When the register output is the digital equivalent of the analog input, the DAC output (v_R) equals v_{in}, and this causes the comparator output to switch to low. With one low input to the AND gate, no clock pulses are passed to the register and counting ceases. The register output is now the digital equivalent of the analog input, and this condition is maintained for the time t_2 until the control input switches to positive once again.



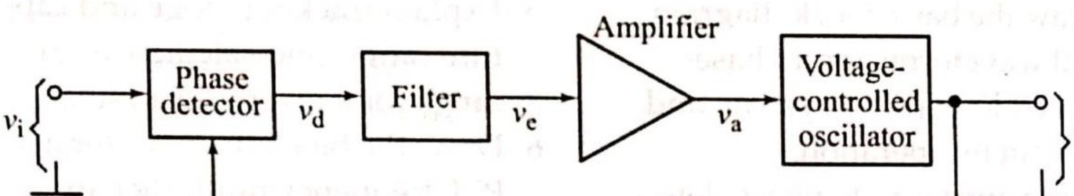
(a) ADC using a digital ramp generator



(b) Waveforms for digital ramp generator ADC

Figure 15-18 Block diagram and waveforms for a digital

Q.7



(a) Basic phase-locked loop block diagram

COMPONENTS OF PLL:

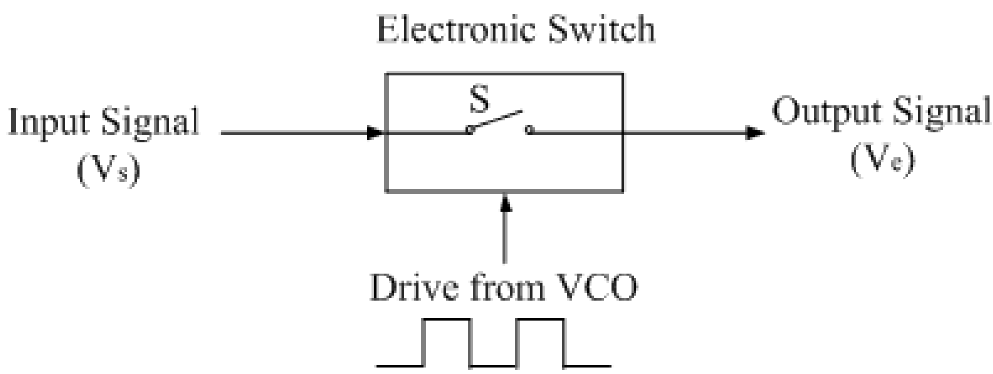
- VOLTAGE CONTROLLED OSCILLATOR (VSO)
- PHASE DETECTOR
- LOW PASS FILTERS

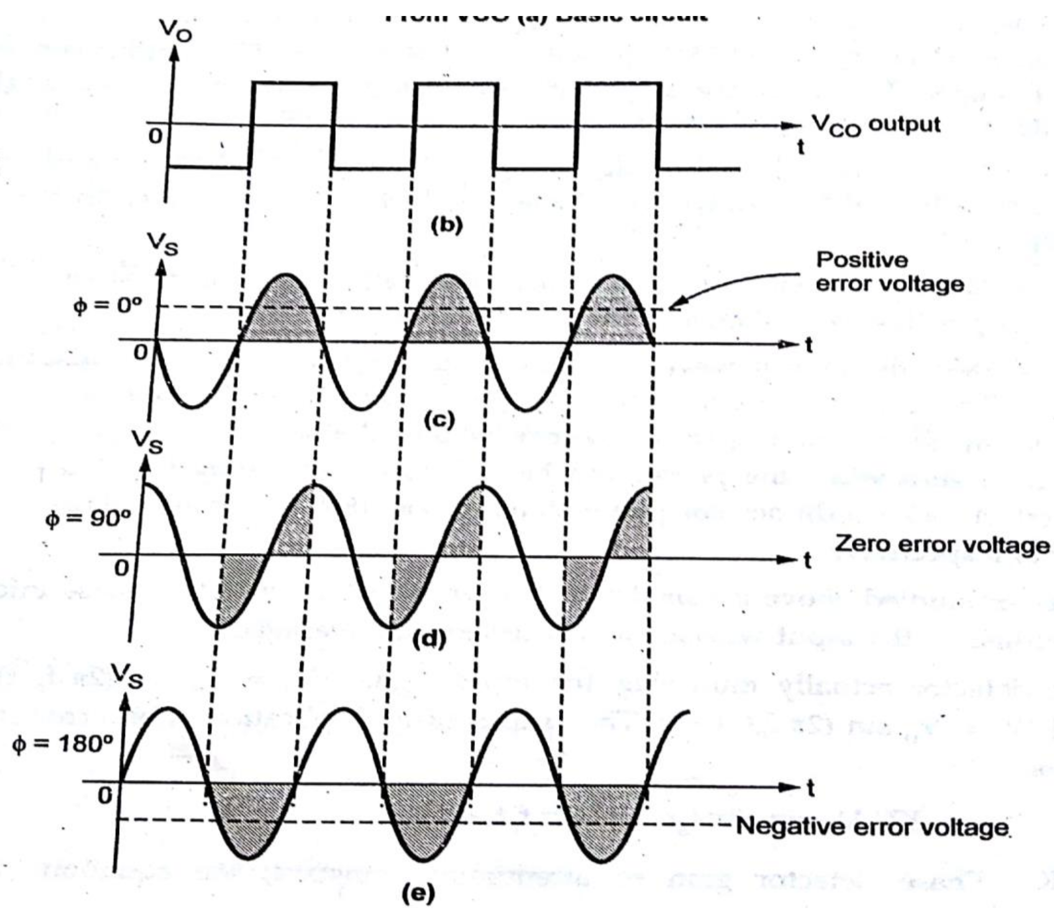
TYPES OF PHASE DETECTOR

1. ANALOG PHASE DETECTOR
2. DIGITAL PHASE DETECTOR

Types of ANALOG PHASE DETECTOR

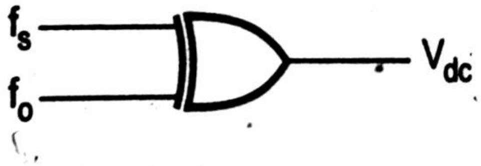
1. ***Switch type***

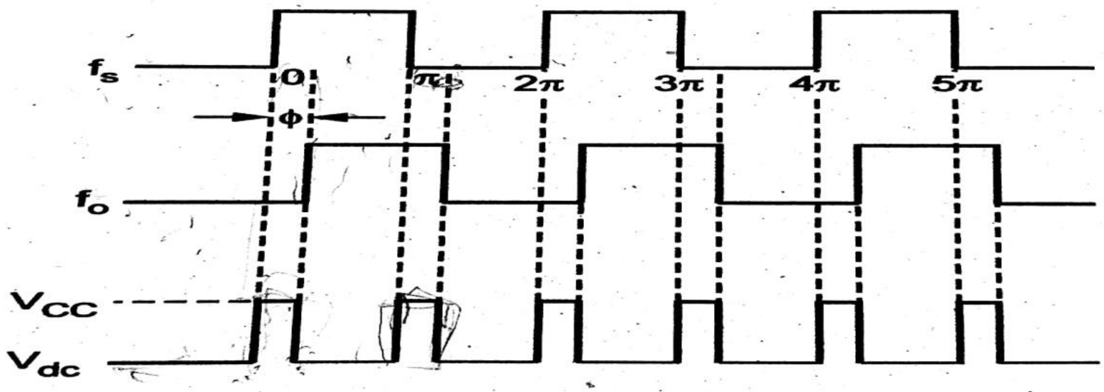


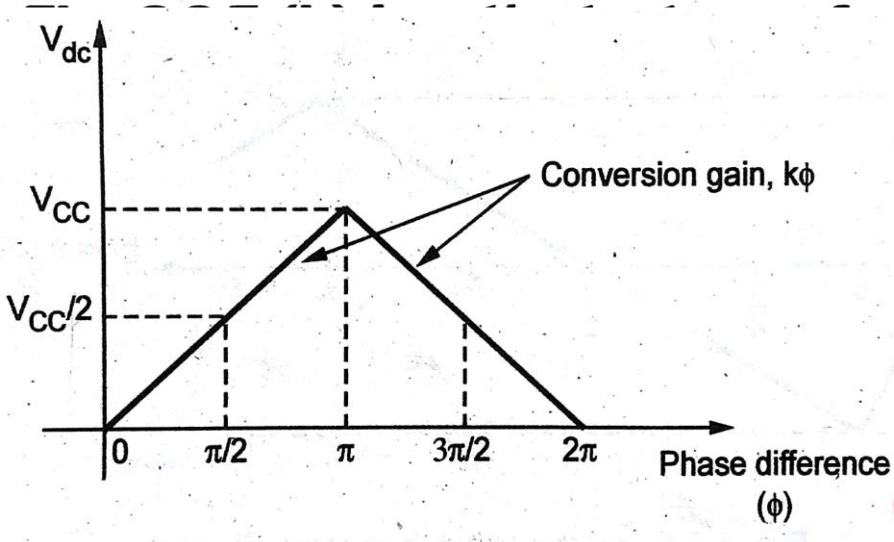


DIGITAL PHASE DETECTOR:

1. Using xor gate







2. ***Using SR flip flop***

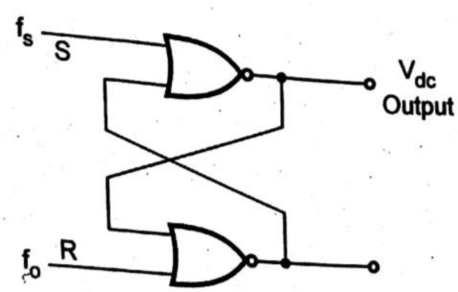


Fig. 8.3.8 (a) Digital phase detector using SR flip-flop

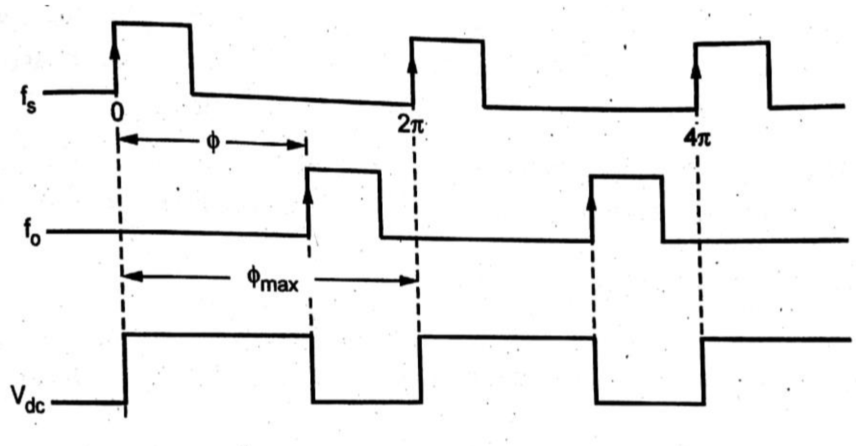
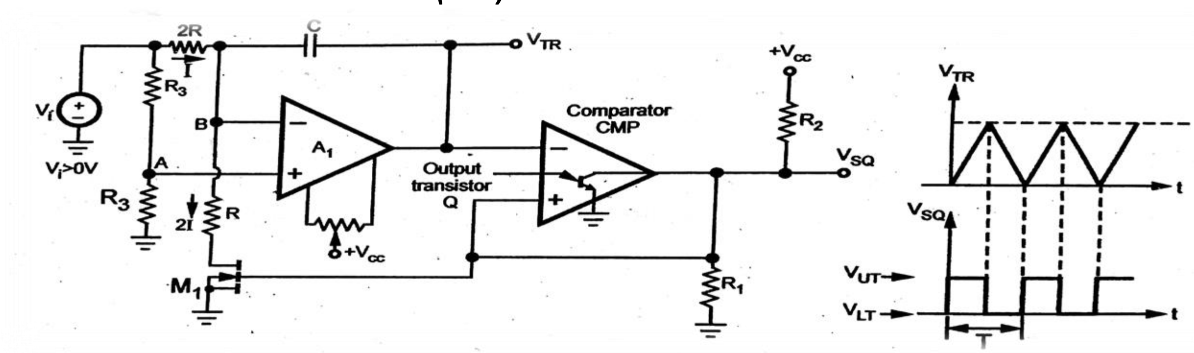


Fig. 8.3.8 (b) Input and output waveforms

VOLTAGE CONTROLLED OSCILLATOR (VSO)



LOW PASS FILTER

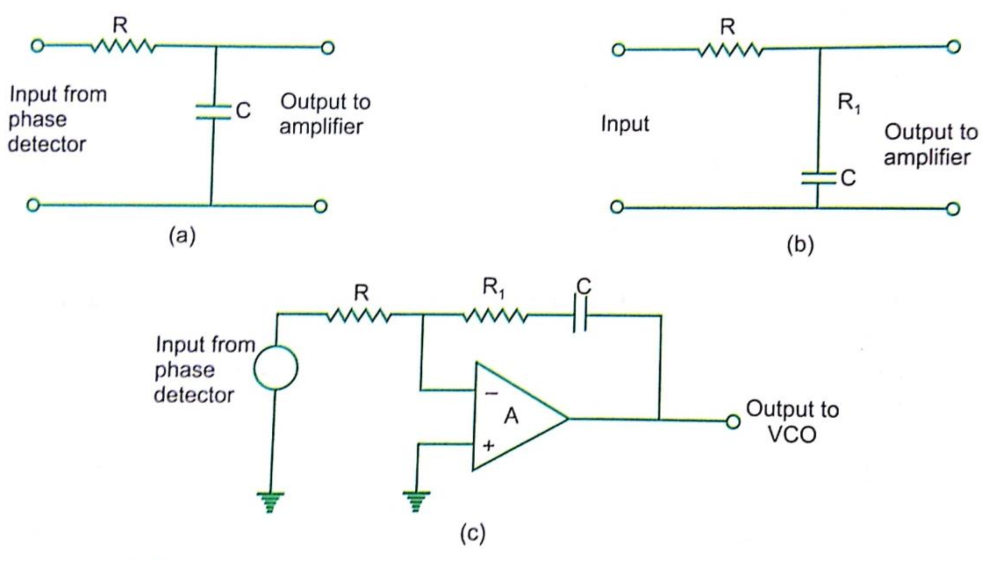
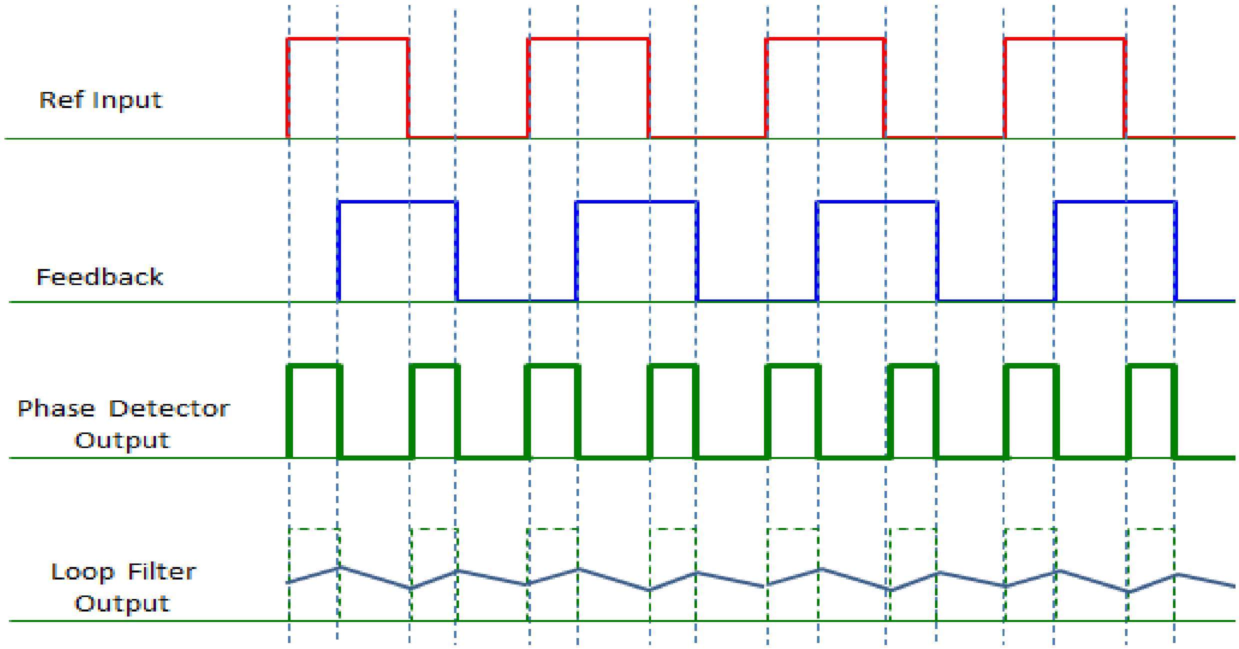
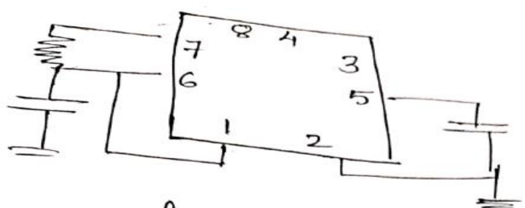


Fig. 9.8 (a) Low pass filter (b) Passive filter (c) Active filter





$$f = \frac{1.45}{(R_A+2R_B)C}$$

$C = 0.1\mu F$

$$f = \frac{1.45}{(R_A+2R_B)C} = 100Hz$$

$$\frac{1.45}{100 \times 0.1 \times 10^{-6}} = R_A + 2R_B$$

$$145k\Omega = R_A + 2R_B \longrightarrow (1)$$

$$\text{Duty cycle } D = \frac{R_A+R_B}{R_A+2R_B}.$$

$$0.75 \times 145K = R_A + R_B$$

$$108.75K = R_A + R_B \longrightarrow (2)$$

$\boxed{R_A = 72.5\,k\Omega \quad R_B = 36.25}$

Standard

$\boxed{R_A = 68k\Omega \quad R_B = 33k\Omega}$