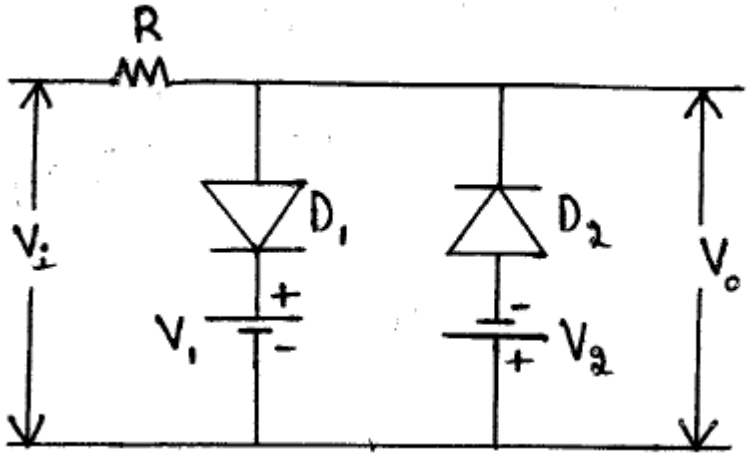
VTU QP SOLUTION- 2018-19 May-AEC-17EE34

1a. Draw a double ended clipper circuit and explain its working principle with transfer characteristics.



During +ve half cycle

* Diode D_2 is always reverse bias & acts as open CKt.

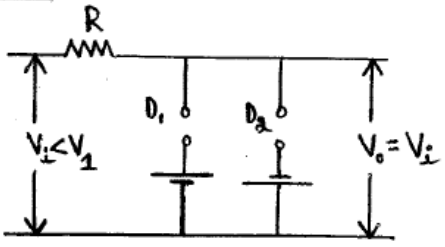
Case i: When $V_i < V_1$, diode D_1 is reverse bias & acts as open CKt.

Thus o/p $\boxed{V_o = V_i}$

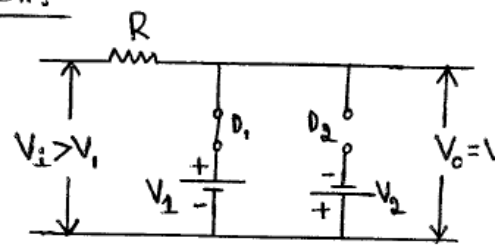
Case ii: When $V_i > V_1$, diode D_1 is forward bias & acts as Short CKt.

Thus o/p $\boxed{V_o = V_1}$

Case i:



Case ii:



During -ve half cycle

* Diode D_1 is always reverse bias & acts as open CKt.

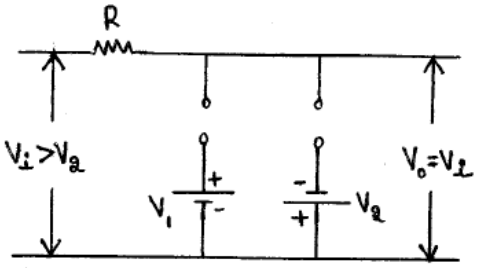
Case i : When $V_i > V_2$, diode D_2 is reverse bias & acts as open CKt.

Thus o/p $\boxed{V_o = V_i}$

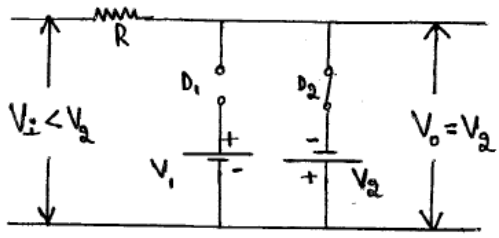
Case ii : When $V_i < V_2$, diode D_2 is forward bias & acts as Short CKt.

Thus o/p $\boxed{V_o = V_2}$

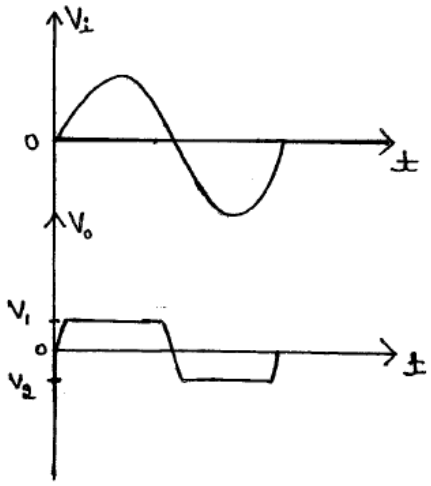
Case i :



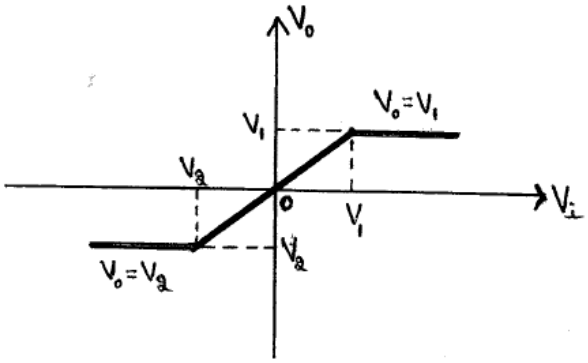
Case ii :



I/o Waveforms :



Transfer characteristics :



1b. Draw and explain the working of clamper circuit which clamps the positive peak of a signal to zero.

* A -ve clamper is a CKt which adds -ve DC voltage to the I/p Signal.

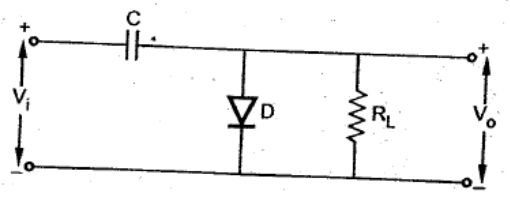


Fig ①

Step 1 :

Find the capacitor voltage when the diode is Conducting (ON).

* During +ve half cycle, diode 'D' is forward biased & Conducts. Now Capacitor 'C' charges with the polarity as shown in Fig ②.

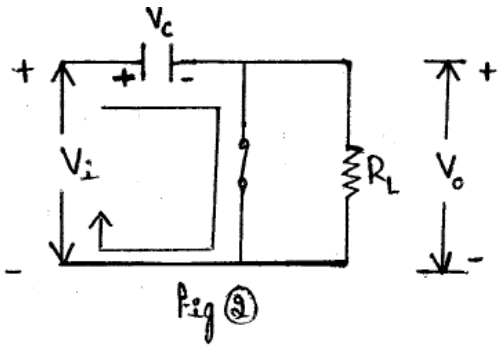


Fig ②

Applying KVL to the CKt, we get

$$V_i - V_c = 0$$

$$V_c = V_i$$

Now $V_i = V_m$

$$\boxed{V_c = V_m} \longrightarrow ①$$

Step 2 :-

Find the o/p voltage when diode is OFF.

* During -ve half cycle, diode 'D' is reverse biased & acts as open circuit & its equivalent CKt is shown in Fig ③

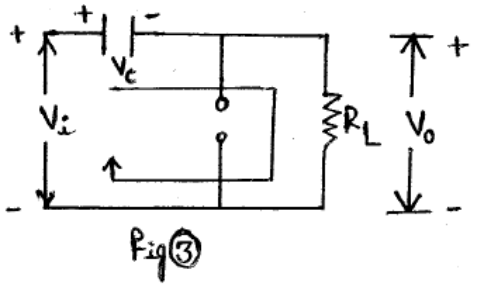


Fig ③

Applying KVL to the CKt, we get

$$V_i - V_c - V_o = 0$$

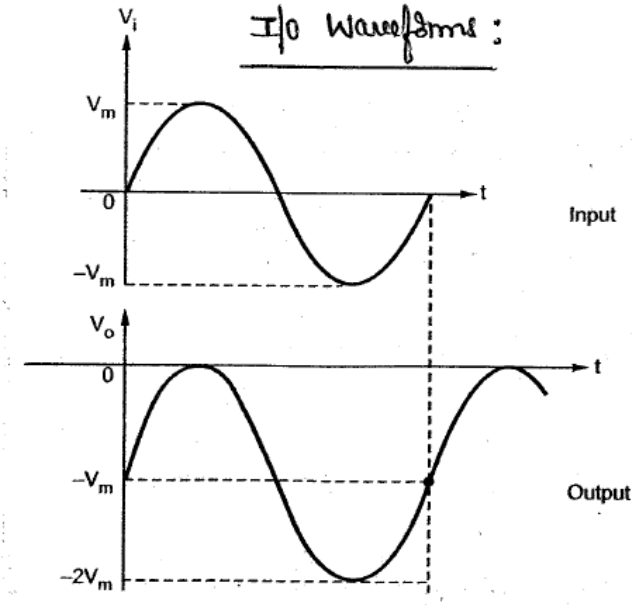
$$\boxed{V_o = V_i - V_c} \longrightarrow ②$$

Substituting eq ① in eq ②, we get

$$\boxed{V_o = V_i - V_m}$$

o/p voltage :

For V_i	$V_o = V_i - V_m$
0	$V_o = -V_m$
V_m	$V_o = 0$
$-V_m$	$V_o = -2V_m$



1c. With suitable graph, explain the significance of operating point.

WKT the load line is constructed on the output characteristics.

❖ **Effect of I_B :-**

If the value of **I_B** is **changed** by **varying** the **value** of **R_B**,the **Q-point moves up** or **down** the **load-line** as shown in figure1.

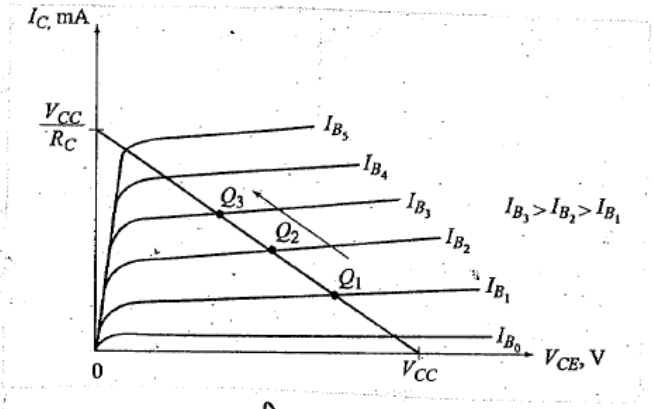


Fig ①

❖ Effect of V_{CC} :-

If **R_C** is **fixed** and **V_{CC} varied**, the load line shifts as shown in figure2. Now the **Q-point varies horizontally** on the **I_{BQ}** line.

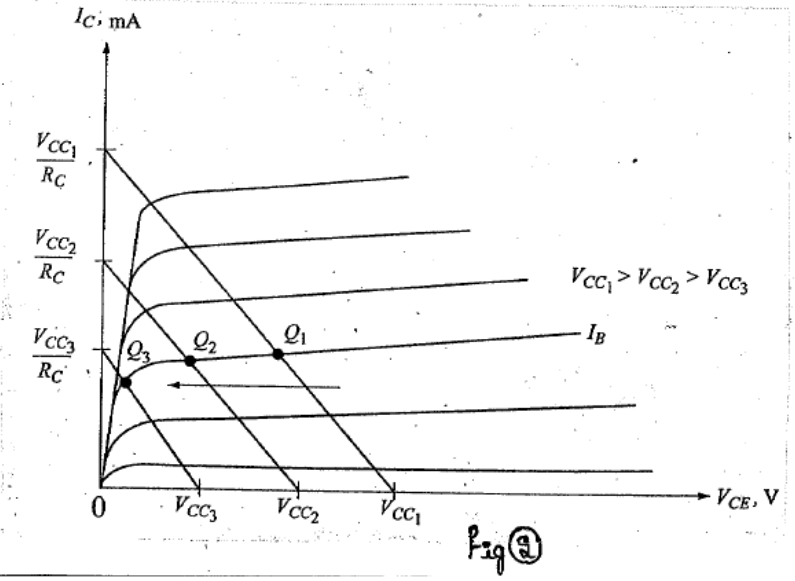


Fig ②

❖ Effect of R_C :-

If **V_{CC}** is kept **constant** and **R_C** is **changed,** keeping base current **I_B fixed,** the **Q-point moves** to the **left into saturation** as shown in figure3.

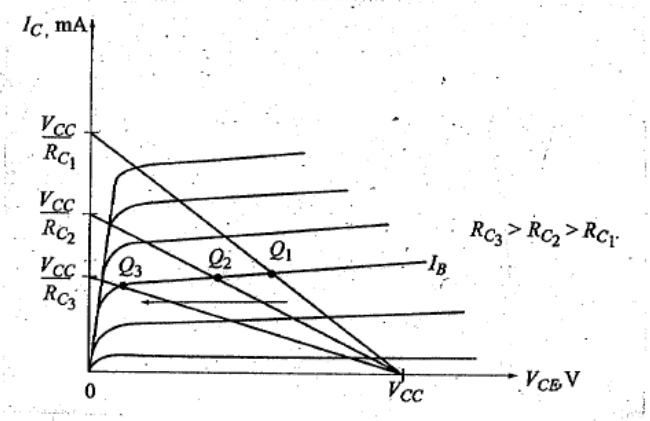


Fig ③

2a. Derive the expression for stability factor for fixed bias circuit, with respect I_{co}, V_{BE} and β.

1) Fixed - Bias circuit :-

1) For fixed-bias ckt, the base current is given by

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \rightarrow (1).$$

Differentiating eq 1 w.r.to I_C, we get

$$\frac{dI_B}{dI_C} = 0 \rightarrow (2).$$

Sub eq (2) in stability factor equation

$$S = \frac{(1+\beta)}{1 - \beta\left(\frac{dI_B}{dI_C}\right)} = \frac{(1+\beta)}{1 - \beta(0)} = \frac{1+\beta}{1}$$

$$\boxed{S = 1+\beta}$$

2) $S' = S(V_{BE}) = \frac{dI_C}{dV_{BE}}$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \rightarrow (1).$$

W.K.T $I_C = \beta I_B \rightarrow (2)$

Sub eq (1) in Eq (2) (I_B value)

$$I_C = \beta \underbrace{\left(\frac{V_{CC} - V_{BE}}{R_B}\right)}_{I_B}$$

$$I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} \rightarrow (3)$$

differentiating eq (3) w.r.to V_{BE}, we get

$$\frac{dI_C}{dV_{BE}} = 0 - (1)\frac{\beta}{R_B} = -\frac{\beta}{R_B}$$

$$\therefore \quad S' = \frac{dI_C}{dV_{BE}} = -\frac{\beta}{R_B}.$$

3) $$S'' = S(\beta) = \frac{dI_C}{d\beta} = \frac{\Delta I_C}{\Delta \beta}.$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} - (1).$$

W.K.T $\beta = \frac{I_C}{I_B}$

$$I_B = \frac{I_C}{\beta}$$

$$\left(\frac{I_C}{\beta}\right) = \frac{V_{CC} - V_{BE}}{R_B}$$

$$\frac{I_C}{\beta} = \frac{V_{CC} - V_{BE}}{R_B}$$

$$\therefore \quad I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right) \rightarrow (2).$$

W.K.T $$S(\beta) = \frac{\Delta I_C}{\Delta \beta} \rightarrow (3).$$

At temperature T_1 , $\beta = \beta_1$, $I_C = I_{C_1}$

At temperature T_2 , $\beta = \beta_2$, $I_C = I_{C_2}$

Then , eq ② can be written as

$$I_{C_1} = \beta_1 \left(\frac{V_{CC} - V_{BE}}{R_B} \right) \rightarrow ④ .$$

Now $I_{C_2} = \beta_2 \left(\frac{V_{CC} - V_{BE}}{R_B} \right) \rightarrow ⑤ .$

eq ⑤ ÷ eq ④

$$\frac{I_{C_2}}{I_{C_1}} = \frac{\beta_2 (1)}{\beta_1 (1)} \rightarrow ⑥ .$$

Subtracting eq ⑥ by 1 on both sides .

$$\frac{I_{C_2}}{I_{C_1}} - 1 = \frac{\beta_2}{\beta_1} - 1$$

$$\frac{I_{C_2} - I_{C_1}}{I_{C_1}} = \frac{\beta_2 - \beta_1}{\beta_1}$$

$$\frac{\Delta I_C}{I_{C_1}} = \frac{\Delta \beta}{\beta_1}$$

W.K.T.

$\Delta I_C = I_{C_2} - I_{C_1}$

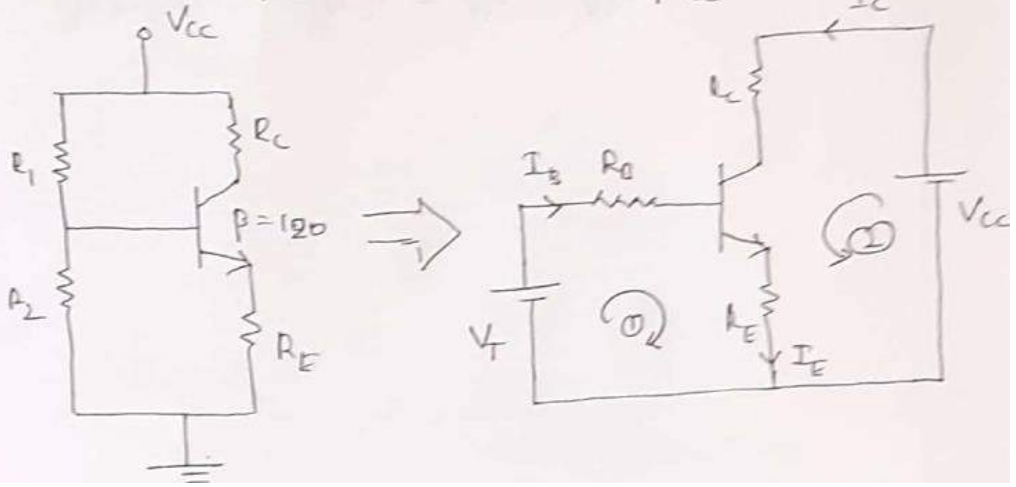
$\Delta \beta = \beta_2 - \beta_1$

$$\therefore \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C_1}}{\beta_1}$$

(07 Marks)

b. A voltage divider biased circuit has $R_1 = 39k\Omega$, $R_2 = 82k\Omega$, $R_C = 3.3k\Omega$, $R_E = 1k\Omega$ and $V_{CC} = 18V$. The Silicon transistor used has $\beta = 120$. Find Q-point and stability factor. (08 Marks)

$R_1 = 39k\Omega$ | $R_2 = 82k\Omega$ | $R_C = 3.3k\Omega$ | $R_E = 1k\Omega$ | $V_{CC} = 18V$



$$V_T = \left[\frac{R_2}{R_1+R_2}\right] V_{CC} = 12.19V \quad \Big| \quad R_B = \frac{R_1 R_2}{R_1+R_2} = 26.43k\Omega$$

KVL to Loop ① $\longrightarrow$ $V_T - I_B R_B - V_{BE} - I_E R_E = 0$

$$V_T - I_B R_B - V_{BE} - (1+\beta) R_E I_B = 0$$

$$I_B = \frac{V_T - V_{BE}}{R_B + (1+\beta) R_E} = \frac{11.49}{147430}$$

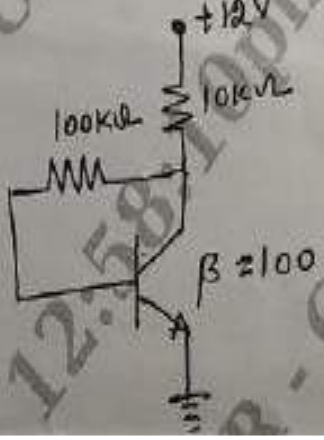
$$I_B = 7.79 \times 10^{-5} A$$

$$\boxed{I_C = \beta I_B = 9.35\,mA}$$

KVL to Loop ② → $V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$.

$V_{CC} - I_C R_C - V_{CE} - (1+\beta) I_B R_E = 0$

c. Calculate the Q point values (I_c and V_{CE}) for the circuit given in Fig Q2(c). (05 Marks)



$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_C} = \frac{12 - 0.7}{100 * 10^3 + (1+100)(10 \times 10^3)} = 10.18\,\mu A$$

$$I_C = \beta I_B = 100 * 10.18\,\mu A = 1.018\,mA$$

$$V_{CE} = V_{CC} - (I_B + I_C) R_C = 1.7182\,V$$

3a. State and prove Miller's theorem.

In general, the Miller theorem is used for converting any circuit having configuration of Fig. 4.48 (a) to another configuration shown in Fig. 4.48 (b).

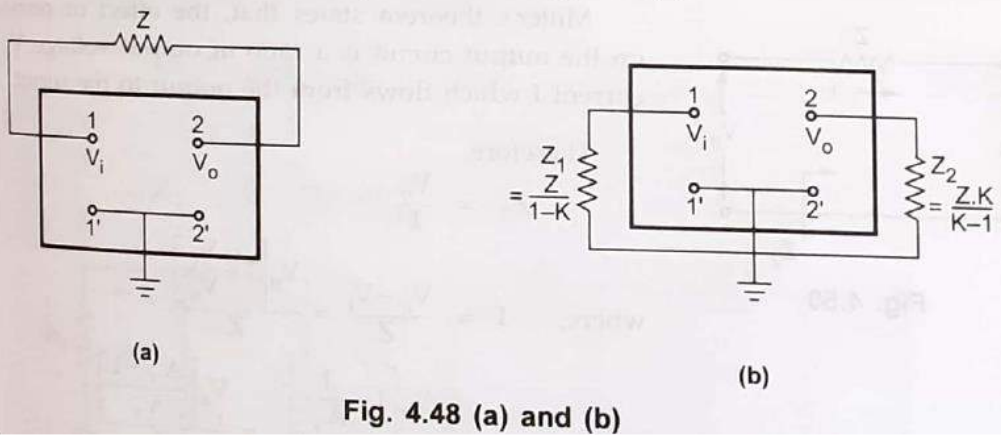


Fig. 4.48 (a) and (b)

Fig. 4.48 (a) and (b)

The Fig. 4.48 shows that, if Z is the impedance connected between two nodes, node 1 and node 2, it can be replaced by two separate impedances Z_1 and Z_2; where Z_1 is connected between node 1 and ground and Z_2 is connected between node 2 and ground.

The V_i and V_o are the voltages at the node 1 and node 2 respectively. The values of Z_1 and Z_2 can be derived from the ratio of V_o and V_i (V_o / V_i), denoted as K. Thus it is not necessary to know the values of V_i and V_o to calculate the values of Z_1 and Z_2.

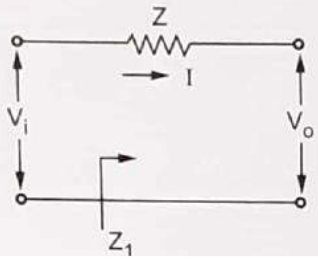
The values of impedances Z_1 and Z_2 are given as

$$Z_1 = \frac{Z}{1-K}$$

and

$$Z_2 = \frac{Z \cdot K}{K-1}$$

4.5.2 Proof of Miller's Theorem



Miller's theorem states that, the effect of resistance Z on the input circuit is a ratio of input voltage V_i to the current I which flows from the input to the output.

Therefore,

$$Z_1 = \frac{V_i}{I}$$

Fig. 4.49

where, $I = \frac{V_i - V_o}{Z} = \frac{V_i\left[1 - \frac{V_o}{V_i}\right]}{Z}$

$= \frac{V_i[1 - A_v]}{Z}$

$\therefore Z_1 = \frac{V_i}{I} = \frac{Z}{1 - A_v} = \frac{Z}{1 - K} \quad \because \frac{V_o}{V_i} = A_v = K$

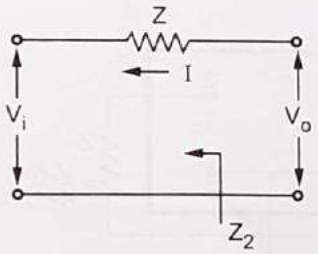


Fig. 4.50

Miller's theorem states that, the effect of resistance Z on the output circuit is a ratio of output voltage V_o to th current I which flows from the output to the input.

Therefore,

$Z_2 = \frac{V_o}{I}$

where, $I = \frac{V_o - V_i}{Z} = \frac{V_o\left[1 - \frac{V_i}{V_o}\right]}{Z}$

$= \frac{V_o\left[1 - \frac{1}{A_v}\right]}{Z} = \frac{V_o\left[\frac{A_v - 1}{A_v}\right]}{Z}$

$\therefore Z_2 = \frac{V_o}{I} = \frac{Z}{\left[\frac{A_v - 1}{A_v}\right]} = \frac{ZA_v}{A_v - 1} = \frac{ZK}{K - 1} \quad \because \frac{V_o}{V_i} = A_v = K$

3b. Starting from fundamentals define h-parameters and obtain h-parameter equivalent circuit of common emitter configuration.

Let us consider transistor amplifier as a black box as shown in the Fig. 4.9.

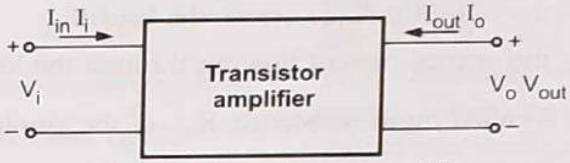


Fig. 4.9 Transistor amplifier

Here, I_i : is the input current to the amplifier

V_i : is the input voltage to the amplifier

I_o : is the output current of the amplifier and

V_o : is the output voltage of the amplifier

As we know transistor is a current operated device, input current is an independent variable. The input current, I_i and output voltage V_o devices the input voltage V_i as well as the output current I_o. Hence input voltage V_i and output current I_o are the dependent variables, whereas input current I_i and output voltage V_o are independent variables. Thus we can write

$V_i = f_1(I_i, V_o)$ ... (1)

$I_o = f_2(I_i, V_o)$ ... (2)

This can be written in the equation form as follows

$$V_i = h_{11} I_i + h_{12} V_o$$

$$I_o = h_{21} I_i + h_{22} V_o$$

The above equations can also be written using alphabetic notations,

$$V_i = h_i \cdot I_i + h_r \cdot V_o$$

$$I_o = h_f \cdot I_i + h_o \cdot V_o$$

Definitions of h-parameter

The parameters in the above equation are defined as follows :

$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0}$ = Input resistance with output short-circuited, in ohms.

$h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i=0}$ = Fraction of output voltage at input with input open circuited.

This parameter is ratio of similar quantities, hence unitless

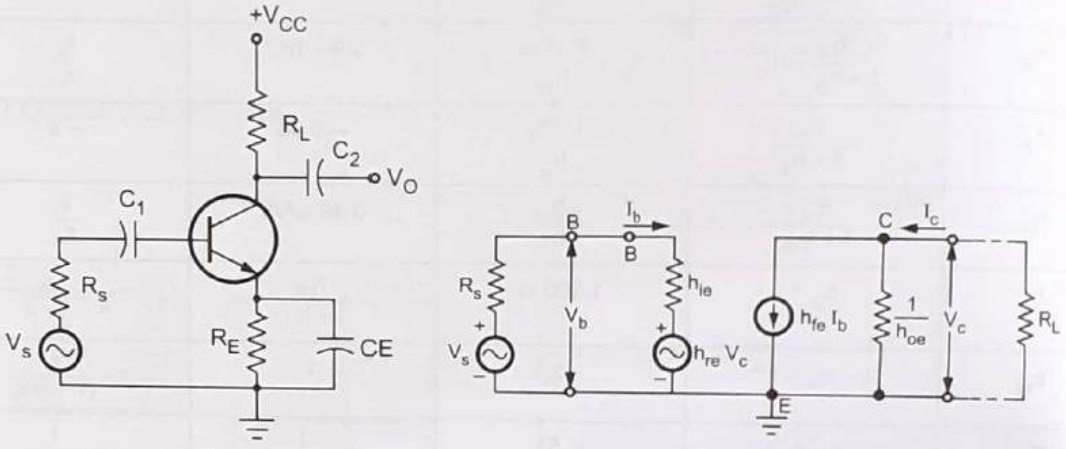
$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0}$ = Forward current transfer ratio or current gain with output short circuited.

This parameter is a ratio of similar quantities, hence unitless.

$h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0}$ = Output admittance with input open-circuited, in mhos.

4.4.1 CE Configuration

Let us consider the common emitter amplifier and it's h-parameter equivalent circuit for the amplifier, as shown in the Fig. 4.34.



(a) CE Configuration

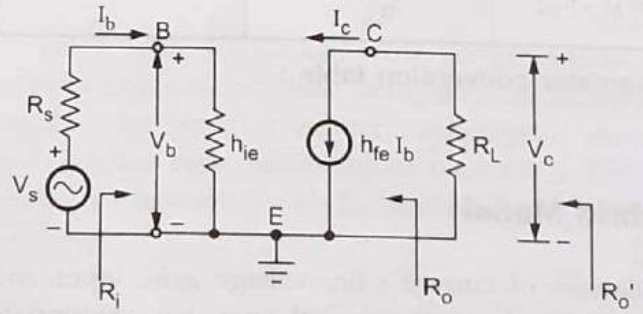
(b) Equivalent Circuit

Fig. 4.34

Since $1/h_{oe}$ is in parallel with R_L and R_C if $1/h_{oe} >> R_L \parallel R_C$, then h_{oe} may be neglected. If we neglect h_{oe}, the collector current I_c is given by $I_c = h_{fe} I_b$. Under these conditions the magnitude of the voltage of the generator in the emitter circuit is,

$$h_{re} |V_{ce}| = h_{re} I_c (R_L \parallel R_C) = h_{re} h_{fe} I_b (R_L \parallel R_C)$$

Since $h_{re} h_{fe} \approx 0.01$, this voltage may be neglected in comparison with the $h_{ie} I_b$ drop across h_{ie}, provided that $R_L \parallel R_C$ is not too large. We therefore conclude that if the load resistance $R_L \parallel R_C$ is small, it is possible to neglect the parameters h_{re} and h_{oe} in the h-parameter equivalent circuit. Fig. 4.35 shows the approximate h-parameter equivalent circuit.



3c. Compare the characteristics of CB,CE and CC configurations.

4.7 Comparison of Transistor Configurations

Sr.No.	Characteristic	Common Base	Common Emitter	Common Collector
1.	Input resistance	Very low (20 Ω)	Low (1 kΩ)	High (500 kΩ)
2.	Output resistance	Very high (1MΩ)	High (40 kΩ)	Low (50 Ω)
3.	Input current	I_E	I_B	I_B
4.	Output current	I_C	I_C	I_E
5.	Input voltage applied between	Emitter and Base	Base and Emitter	Base and Collector
6.	Output voltage taken between	Collector and Base	Collector and Emitter	Emitter and Collector
7.	Current amplification factor	$\alpha = \frac{I_C}{I_E}$	$\beta = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$
8.	Current gain	Less than unity	High (20 to few hundreds)	High (20 to few hundreds)
9.	Voltage gain	Medium	Medium	Low
10.	Applications	As a input stage of multistage amplifier	For audio signal amplification	For impedance matching

4a. Derive an expression for input impedance, voltage gain, current gain and output impedance of emitter follower circuit using h-parameter model for transistor.

b. For the transistor connected in CE configuration, determine A_v, A_i, R_i and R_o using complete hybrid equivalent model. (08 Marks)

Given $R_L = R_C = 1k\Omega$, $h_{ie} = 1k\Omega$, $h_{re} = 2\times10^{-4}$, $h_{fe} = 100$ and $h_{oe} = 20\mu A/V$

c. A transistor in CE mode has h-parameters (08 Marks)

Solution : For CE configuration :

Current gain

$$A_I = \frac{-h_{fe}}{1+h_{oe}R_L} = \frac{-100}{1+20\times10^{-6}\times1\times10^{3}}$$

$$= -98$$

Input resistance

$$R_i = h_{ie}+h_{re}A_iR_L = 1000 + 2\times10^{-4}\times-98\times1000$$

$$= 980.4\ \Omega$$

Voltage gain

$$A_v = \frac{A_iR_L}{R_i} = \frac{-98\times1000}{1000}$$

$$= -98$$

$$Y_o = h_{oe}-\frac{h_{fe}h_{re}}{h_{ie}+R_S} = 20\times10^{-6}-\frac{100\times2\times10^{-4}}{1000+1000}$$

$$= 1.9\times10^{-5}$$

Output resistance

$$R_o = \frac{1}{Y_o} = \frac{1}{1.9\times10^{-5}} = 52.64\ k\Omega$$

c. A transistor in CE mode has h-parameters $h_{ie} = 1.1k\Omega$, $h_{re} = 2\times10^{-4}$, $h_{fe} = 100$ and $h_{oe} = 25\mu A/V$. Determine the equivalent CB parameters. (08 Marks)

(04 Marks)

$$\text{X}\ h_{fc} = \frac{-h_{fb}}{1+h_{fb}} \rightarrow h_{fc}+h_{fc}\cdot h_{fb} = -h_{fb}$$

$$\rightarrow h_{fb}(1+h_{fc}) = -h_{fc}$$

$$\rightarrow h_{fb} = \frac{-h_{fc}}{1+h_{fc}} = -0.99$$

$$\boxed{h_{fb} = -0.99}$$

$$h_{oe} = \frac{h_{ob}}{1 + h_{fb}}$$

$$h_{ob} = h_{oe}(1 + h_{fb}) = 0.25\ \mu A/V$$

$$h_{ie} = \frac{h_{ib}}{1 + h_{fb}}$$

$$h_{ib} = h_{ie}(1 + h_{fb}) = 0.011\ k\Omega$$

$$h_{re} = \frac{h_{ib}h_{ob}}{1 + h_{fb}} - h_{rb}$$

$$h_{rb} = \frac{h_{ib}h_{ob}}{1 + h_{fb}} - h_{re} = 0.274\ V$$

5a. Draw the circuit of Darlington emitter follower. Derive the expression for current gain using its ac equivalent circuit.

AC Equivalent

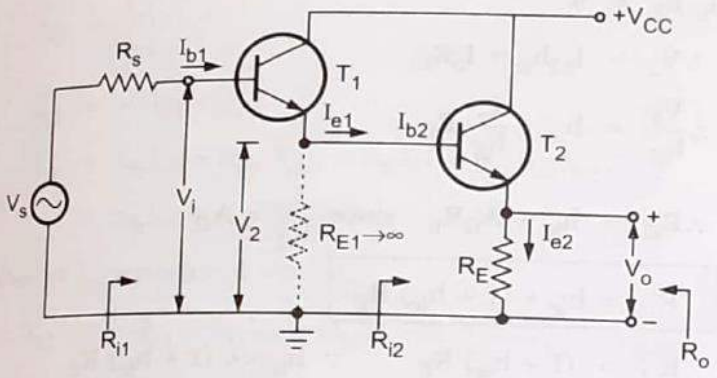


Fig. 6.19 Darlington emitter follower circuit

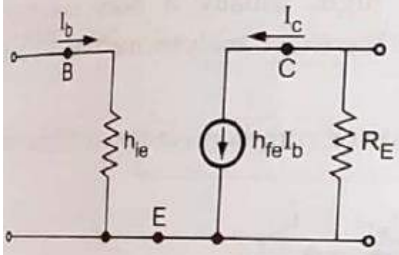


Fig. 6.20

Assume that the load resistance R_L is such that $R_L\ h_{oe} < 0.1$, therefore we can use approximate analysis method for analysing second stage.

Fig. 6.20 shows approximate h-parameter (AC) equivalent circuit for common emitter configuration.

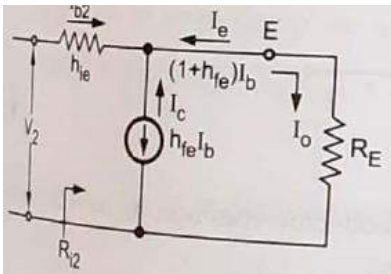


Fig. 6.21

The same circuit can be redrawn by making collector common to have approximate h-parameter equivalent circuit for common collector configuration as shown in Fig. 6.21.

alysis of second stage :

a) Current Gain (A_{i2}) : $A_{i2} = \dfrac{I_o}{I_b} = -\dfrac{I_e}{I_b} = \dfrac{I_b + h_{fe} I_b}{I_b} = \dfrac{I_b(1+h_{fe})}{I_b}$

$\therefore$ $\boxed{A_{i2} = 1 + h_{fe}}$

a) Current Gain (A_{i1}) :

$$A_{i1} = \frac{I_{b2}}{I_{b1}}$$

$$A_{i1} = \frac{I_{e1}}{I_{b1}}$$

$$I_{e1} = -(I_{b1} + I_{c1}) \quad \ldots (4)$$

$$I_{c1} = h_{fe}I_{b1} + h_{oe} V_{ce1} = h_{fe}I_{b1} + h_{oe}(-I_{b2} R_{L1})$$

and

$$= h_{fe}I_{b1} + h_{oe} I_{e1} R_{L1}$$

Substituting value of I_{c1} equation 4 we get,

$$\therefore I_{e1} = -(I_{b1} + h_{fe}I_{b1} + h_{oe} I_{e2} R_{L1}) = -I_{b1} - h_{fe}I_{b1} - h_{oe}I_{e1}R_{L1}$$

$$\therefore I_{e1} + h_{oe}R_{L1}I_{e1} = -I_{b1}(1 + h_{fe})$$

$$-\frac{I_{e1}}{I_{b1}} = \frac{1+h_{fe}}{1+h_{oe}R_{L1}}$$

We know that, $R_{L1} = (1 + h_{fe}) R_E$

$$\therefore \boxed{A_{i1} = -\frac{I_{e1}}{I_{b1}} = \frac{1+h_{fe}}{1+h_{oe}(1+h_{fe})R_E}} \quad \ldots (5)$$

$$= \frac{1+h_{fe}}{1+h_{oe}h_{fe}R_E} \quad \because h_{fe} >> 1$$

5b. What are the advantages of negative feedback amplifiers. Explain briefly.

5c. For voltage series feedback amplifier, derive an expression for output impedance.

7.3.1.7 Output resistance

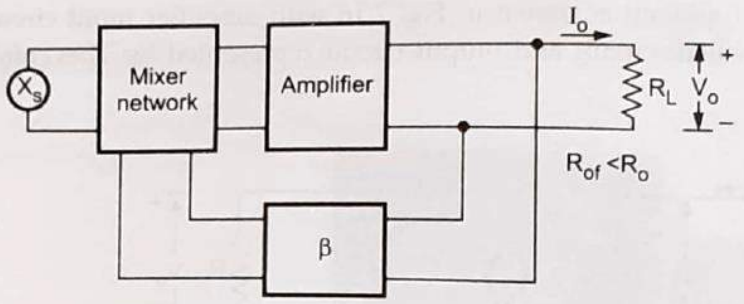


Fig. 7.17

The negative feedback which samples the output voltage, regardless of how this output signal is returned to the input, tends to decrease the output resistance, as shown in the Fig. 7.17.

On the other hand, the negative feedback which samples the output current, regardless of how this output signal is returned to the input, tends to increase the output resistance, as shown in the Fig. 7.18.

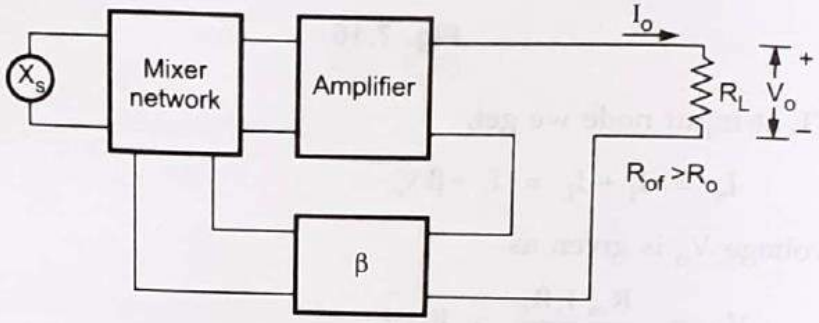
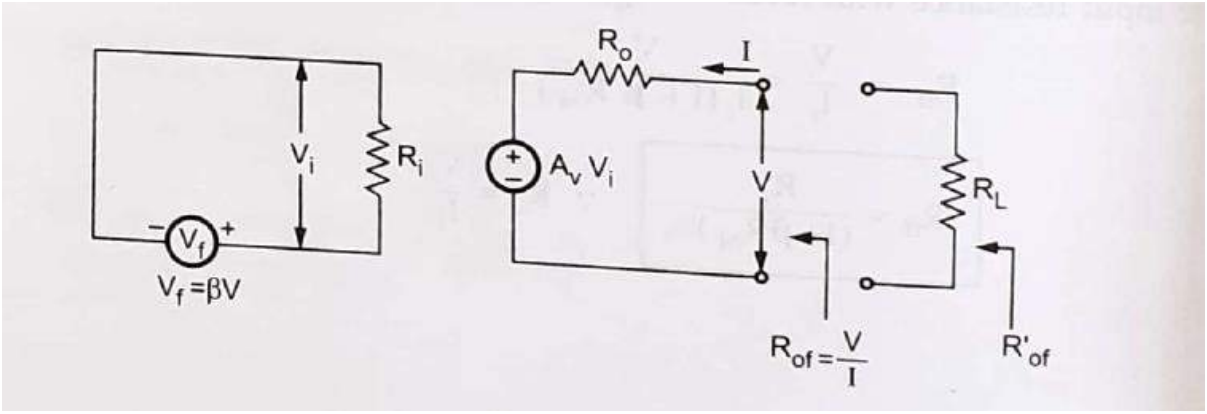


Fig. 7.18

Now, we see the effect of negative feedback on output resistance in different topologies (ways) of introducing negative feedback and obtain R_{of} quantitatively.

Voltage series feedback

In this topology, the output resistance can be measured by shorting the input source $V_s = 0$ and looking into the output terminals with R_L disconnected, as shown in the Fig. 7.19.



Applying KVL to the output side we get,

$$A_v V_i + IR_o - V = 0$$

$$I = \frac{V - A_v V_i}{R_o}$$

$\therefore$ The input voltage is given as

$$V_i = -V_f = -\beta V \quad \because V_s = 0 \qquad \ldots (33)$$

Substituting the V_i from equation (33) in equation (32) we get,

$$I = \frac{V + A_v \beta V}{R_o}$$

$$= \frac{V(1 + \beta A_v)}{R_o}$$

$$R_{of} = \frac{V}{I} = \frac{R_o}{(1 + \beta A_v)} \qquad \ldots (34)$$

Note : Here A_v is the open loop voltage gain without taking R_L in account,

$$R'_{of} = R_{of} \parallel R_L$$

$$= \frac{R_{of} \times R_L}{R_{of} + R_L} = \frac{\left(\frac{R_o}{1+\beta A_v}\right) \times R_L}{\frac{R_o}{(1+\beta A_v)} + R_L}$$

$$= \frac{R_o R_L}{R_o + R_L(1+\beta A_v)} = \frac{R_o R_L}{R_o + R_L + \beta A_v R_L}$$

Dividing numerator and denominator by $(R_o + R_L)$ we get

$$R'_{of} = \frac{\frac{R_o R_L}{R_o + R_L}}{1 + \frac{\beta A_v R_L}{R_o + R_L}}$$

$R_o + R_L$

$$\therefore \quad \boxed{R'_{of} = \frac{R'_L}{1+\beta A_v}} \quad \because R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } A_v = \frac{A_v R_L}{R_o + R_L} \quad \ldots$$

Note : Here A_v is the open loop voltage gain taking R_L into account.

6a. Explain the need of cascading amplifier. Draw and explain the block diagram of two stage cascade amplifier.

design of multistage amplifiers.

6.1.1 Need for Cascading

For faithful amplification amplifier should have desired voltage gain, current gain and it should match its input impedance with the source and output impedance with the load. Many times these primary requirements of the amplifier cannot be achieved with single stage amplifier, because of the limitation of the transistor/FET parameters. In such situations more than one amplifier stages are cascaded such that input and output stages provide impedance matching requirements with some amplification and remaining middle stages provide most of the amplification.

In short we can say that,

- When the amplification of a single stage amplifier is not sufficient, or,
- When the input or output impedance is not of the correct magnitude, for a particular application two or more amplifier stages are connected, in cascade. Such amplifier, with two or more stages is also known as multistage amplifier.

... also known as multistage amplifier.

6.2 Cascade Connections

6.2.1 Two Stage Cascaded Amplifier

Fig. 6.1 shows the block diagram of two stage cascaded amplifier. These stages are connected such that the output of the first stage is connected to the input of the second stage.

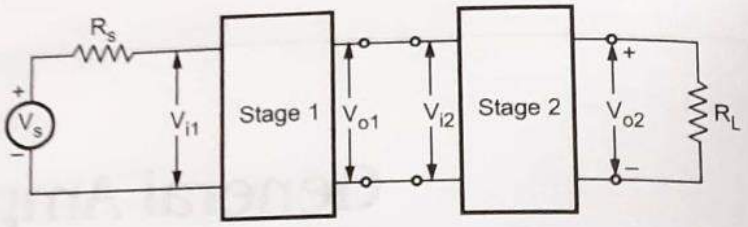


Fig. 6.1 Block diagram of two stage cascade amplifier

As shown in the Fig. 6.1 V_{i1} is the input of the first stage and V_{o2} is the output of the second stage. Therefore V_{o2}/V_{i1} is the overall voltage gain of two stage amplifier and it can be given as,

$$A_V = \frac{V_{o2}}{V_{i1}}$$

$$= \frac{V_{o2}}{V_{i2}} \frac{V_{i2}}{V_{i1}}$$

We know that, $V_{o1} = V_{i2}$

$$\therefore A_V = \frac{V_{o2}}{V_{i2}} \frac{V_{o1}}{V_{i1}}$$

$$= A_{V2} A_{V1}$$

So that, we can say the voltage gain of multistage amplifier is the product of voltage gains of the individual stages.

In the block diagram of two-stage amplifier we have not considered the biasing arrangements for simplicity. Now, with primary understanding we will see the two stage amplifier with biasing arrangements and we will analyse its performance with the help of h-parameters.

b. A given amplifier arrangement has the following voltage gains $A_{V_1} = 10$, $A_{V_2} = 20$ and $A_{V_3} = 40$. Calculate the overall voltage gain and determine the total voltage gain in dBs. (06 Marks)

$$A_V = A_{V_1} \cdot A_{V_2} \cdot A_{V_3}$$

$$= 10 * 20 * 40 = 8000$$

$$A_{V_1}(dB) = 20 \log 10 = 20$$

$$A_{V_2}(dB) = 20 \log 20 = 26$$

$$A_{V_3}(dB) = 20 \log 40 = 32$$

$$A_V(dB) = A_{V_1}(dB) + A_{V_2}(dB) + A_{V_3}(dB) = 78 dB.$$

c. An amplifier with negative feedback has a voltage gain of 120. It is found that without feedback an input signal of 60mV is required to produce a particular output, whereas with feedback the input signal must be 0.5V to get the same output. Find voltage gain (A_V) and β of the amplifier. **(06 Marks)**

(06 Marks)

Given $A_{Vf} = 120$

$$A_V = \frac{V_o}{V_s} = \frac{V_o}{60mV}$$

And $A_{Vf} = \frac{V_o}{0.5} \rightarrow V_o = 0.5 * 120 = 60V$

$$\therefore \boxed{A_V = \frac{V_o}{V_s} = \frac{60}{60mV} = 1000}$$

From $A_{vf} = \frac{A_v}{1 + A_v\beta} \rightarrow \boxed{\beta = 0.00733}$

7a. Derive an expression for frequency of oscillations of Wien Bridge oscillator.

9.6 Wien Bridge Oscillator

Generally in an oscillator, amplifier stage introduces 180° phase shift and feedback network introduces additional 180° phase shift, to obtain a phase shift of 360° (2π radians) around a loop. This is required condition for any oscillator. But Wien bridge oscillator uses a noninverting amplifier and hence does not provide any phase shift during amplifier stage. As total phase shift required is 0° or 2 $n\pi$ radians, in Wien bridge type no phase shift is necessary through feedback. Thus the total phase shift around a loop is 0°. Let us study the basic version of the Wien bridge oscillator and its analysis.

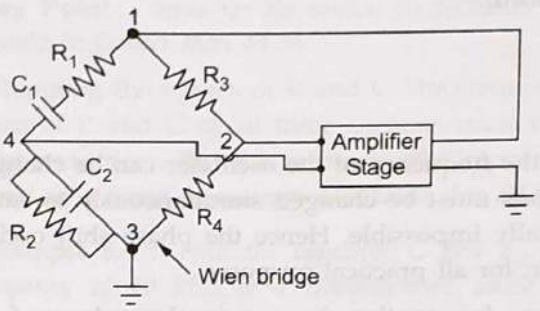


Fig. 9.12 Basic circuit of Wien bridge oscillator

A basic Wien bridge used in this oscillator and an amplifier stage is shown in the Fig. 9.12.

The output of the amplifier is applied between the terminals 1 and 3, which is the input to the feedback network. While the amplifier input is supplied from the diagonal terminals 2 and 4, which is the output from the feedback network. Thus amplifier supplied its own input through the Wien bridge as a feedback network.

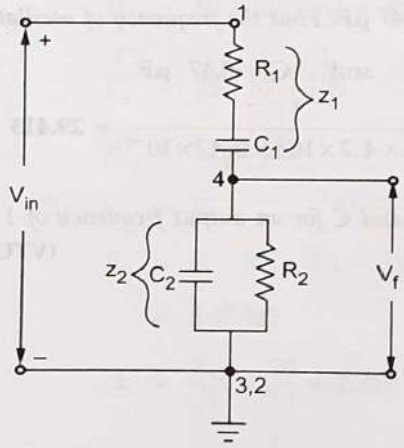


Fig. 9.13 Feedback network of Wien bridge oscillator

The two arms of the bridge, namely R_1, C_1 in series and R_2, C_2 in parallel are called **frequency sensitive arms**. This is because the components of these two arms decide the frequency of the oscillator. Let us find out the gain of the feedback network. As seen earlier input V_{in} to the feedback network is between is 1 and 3 while output V_f of the feedback network is between 2 and 4. This is shown in the Fig. 9.13. Such a feedback network is called **lead-lag network**. This is because at very low frequencies it acts like a lead while at very high frequencies it acts like lag network.

9.6.1 Derivation for Frequency of Oscillations

Now from the Fig. 9.13, as shown,

$$Z_1 = R_1 + \frac{1}{j\omega C_1} = \frac{1 + j\omega R_1 C_1}{j\,\omega\, C_1}$$

$$Z_2 = R_2 \parallel \frac{1}{j\omega C_2} = \frac{R_2 \times \frac{1}{j\,\omega C_2}}{R_2 + \frac{1}{j\omega C_2}}$$

$$= \frac{R_2}{1 + j\omega R_2 C_2} \quad \ldots (1)$$

Replacing $j\omega = s$,

$$Z_1 = \frac{1 + s R_1 C_1}{s C_1}$$

and

$$Z_2 = \frac{R_2}{1 + s R_2 C_2}$$

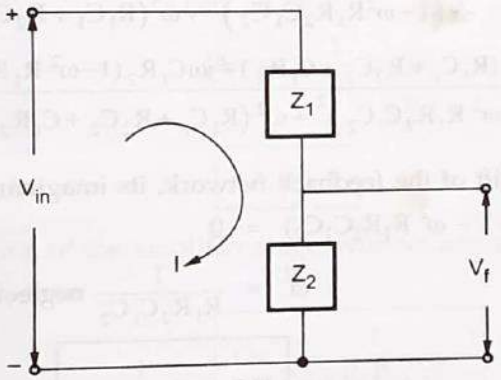


Fig. 9.14 Simplified circuit

$$I = \frac{\text{in}}{Z_1 + Z_2}$$

$$V_f = I\, Z_2$$

$$V_f = \frac{V_{in}\, Z_2}{Z_1 + Z_2}$$

$$\boxed{\beta = \frac{V_f}{V_{in}} = \frac{Z_2}{Z_1 + Z_2}}$$

Substituting the values of Z_1 and Z_2,

$$\beta = \frac{\left[\frac{R_2}{1+sR_2C_2}\right]}{\left[\frac{1+sR_1C_1}{sC_1}\right]+\left[\frac{R_2}{1+sR_2C_2}\right]}$$

$$\beta = \frac{s C_1 R_2}{(1+s R_1 C_1)(1+s R_2 C_2)+s C_1 R_2}$$

$$= \frac{s C_1 R_2}{1+s(R_1 C_1 + R_2 C_2)+s^2 R_1 R_2 C_1 C_2 + s C_1 R_2}$$

$$= \frac{s C_1 R_1}{1+s(R_1 C_1 + R_2 C_2 + C_1 R_2)+s^2 R_1 R_2 C_1 C_2}$$

Replacing s by $j\omega$, $s^2, = -\omega^2$

$$\therefore \quad \beta = \frac{j\omega C_1 R_2}{(1-\omega^2 R_1 R_2 C_1 C_2)+j\omega(R_1 C_1 + R_2 C_2 + C_1 R_2)} \quad \ldots (3)$$

Rationalising the expression,

$$\beta = \frac{j\omega C_1 R_2 \left[(1-\omega^2 R_1 R_2 C_1 C_2) - j\omega(R_1 C_1 + R_2 C_2 + C_1 R_2)\right]}{\left(1-\omega^2 R_1 R_2 C_1 C_2\right)^2 + \omega^2 (R_1 C_1 + R_2 C_2 + C_1 R_2)^2}$$

$$\beta = \frac{\omega^2 C_1 R_2 (R_1 C_1 + R_2 C_2 + C_1 R_2)+j\omega C_1 R_2 (1-\omega^2 R_1 R_2 C_1 C_2)}{\left(1-\omega^2 R_1 R_2 C_1 C_2\right)^2 + \omega^2 (R_1 C_1 + R_2 C_2 + C_1 R_2)^2} \quad \ldots (4)$$

To have zero phase shift of the feedback network, its imaginary part must be zero.

$$\therefore \quad \omega(1 - \omega^2 R_1 R_2 C_1 C_2) = 0$$

$$\therefore \quad \omega^2 = \frac{1}{R_1 R_2 C_1 C_2} \text{ neglecting zero value.}$$

$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}}$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}} \quad \ldots (5)$$

This is the frequency of the oscillator and it shows that the components of the quency sensitive arms are the deciding factors, for the frequency.

In practice, $R_1 = R_2 = R$ and $C_1 = C_2 = C$ are selected.

$$\therefore \quad f = \frac{1}{2\pi\sqrt{R^2 C^2}}$$

7b. Explain the operation of class B push pull amplifier. Prove that the maximum efficiency of class B configuration is 78.5%.

8.11 Push Pull Class B Amplifier

The push pull circuit requires two transformers, one as input transformer called **driver transformer** and the other to connect the load called **output transformer**. The input signal is applied to the primary of the driver transformer. Both the transformers are centre tapped transformers. The push pull class B amplifier circuit is shown in the Fig. 8.25.

In the circuit, both Q_1 and Q_2 transistors are of n-p-n type. The circuit can use both Q_1 and Q_2 of p-n-p type. In such a case, the only change is that the supply voltage must be $-V_{CC}$, the basic circuit remains the same. Generally the circuit using n-p-n transistors is used. Both the transistors are in common emitter configuration.

The driver transformer drives the circuit. The input signal is applied to the primary of the driver transformer. The centre tap on the secondary of the driver transformer is grounded. The centre tap on the primary of the output transformer is connected to the supply voltage + V_{CC}.

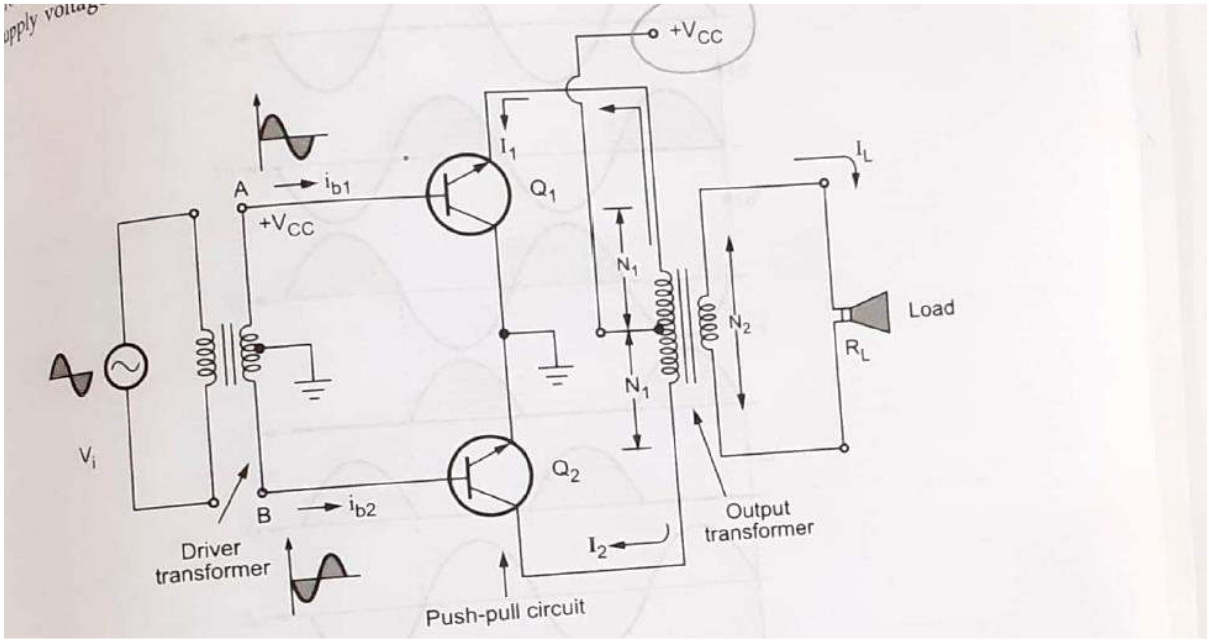


Fig. 8.25 Push pull class B amplifier

With respect to the centre tap, for a positive half cycle of input signal, the point A shown on the secondary of the driver transformer will be positive. While the point B will be negative. Thus the voltages in the two halves of the secondary of the driver transformer will be equal but with opposite polarity. Hence the input signals applied to the base of the transistors Q_1 and Q_2 will be 180° out of phase.

The transistor Q_1 conducts for the positive half cycle of the input producing positive half cycle across the load. While the transistor Q_2 conducts for the negative half cycle of the input producing negative half cycle across the load. Thus across the load, we get a full cycle for a full input cycle. The basic push pull operation is shown in the Fig. 8.26.

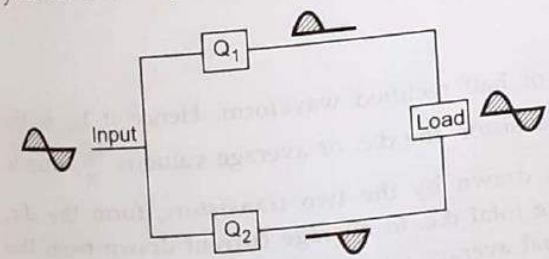


Fig. 8.26 Basic push pull operation

When point A is positive, the transistor Q_1 gets driven into an active region while the transistor Q_2 is in cut-off region. While when point A is negative, the point B is positive, hence the transistor Q_2 gets driven into an active region while the transistor Q_1 is in cut-off region.

8.11.5 Efficiency

The efficiency of the class B amplifier can be calculated using the basic equation.

$$\% \eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{\left(\frac{V_m I_m}{2}\right)}{\frac{2}{\pi} V_{CC} I_m} \times 100$$

$$\therefore \quad \boxed{\% \eta = \frac{\pi}{4} \frac{V_m}{V_{CC}} \times 100} \qquad \ldots (7)$$

8.11.6 Maximum Efficiency

From the equation (7), it is clear that as the peak value of the collector voltage V_m increases, the efficiency increases. The maximum value of V_m possible is equal to V_{CC} as shown in the Fig. 8.30.

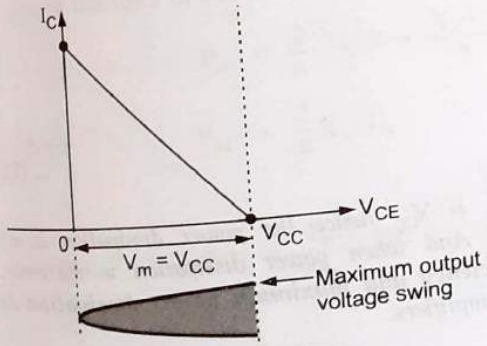


Fig. 8.30

$$\boxed{V_m = V_{CC} \text{ for maximum } \eta}$$

$$\therefore \%\,\eta_{max} = \frac{\pi}{4} \times \frac{V_{CC}}{V_{CC}} \times 100$$

$$= 78.5\ \%$$

Key Point: *Thus the maximum possible theoretical efficiency in case of push pull class B amplifier is 78.5 % which is much higher than the transformer coupled class A amplifier.*

For practical circuits it is upto 65 to 70 %.

Key Point : *Practically the collector-emitter voltage of transistor is neglected as small. But if $V_{CE(min)}$ is given then maximum collector voltage V_m reduces by $V_{CE(min)}$ and becomes $V_m = V_{CC} - V_{CE(min)}$ under maximum efficiency condition.*

8.11.7 Power Dissipation

The power dissipation by both the transistors is the difference between a.c. power output and d.c. power input.

$$\therefore \quad P_d = P_{DC} - P_{ac} = \frac{2}{\pi} V_{CC} I_m - \frac{V_m I_m}{2}$$

c. A crystal has following parameters. L = 0.3344H, C = 0.065pF, C_m = 1pF and R = 5.5kΩ. Calculate: i) Series resonance frequency ii) Parallel resonance frequency. **(08 Marks) (04 Marks)**

$L = 0.3344H \mid C = 0.065 \times 10^{-12}F \mid C_m = 1 \times 10^{-12}F$

$R = 5.5k\Omega$

$$f_s = \frac{1}{2\pi\sqrt{LC}} = 1.08\ MHz$$

$$C_{eq} = \frac{C_m C}{C_m + C} = 0.06458 \times 10^{-2}F$$

$$f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} = 1.084\ MHz$$

8a. Explain the operation of class A transformer coupled power amplifier and prove that the maximum efficiency of is 50%.

8.8 Transformer Coupled Class A Amplifier

As stated earlier, for maximum power transfer to the load, the impedance matching i necessary. For loads like loudspeaker, having low impedance values, impedance matchin is difficult using directly coupled amplifier circuit. This is because loudspeaker resistance i in the range of 3 to 4 ohms to 16 ohms while the output impedance of series fed directl coupled class A amplifier is very much high. This problem can be eliminated by using transformer to deliver power to the load.

Key Point: *The transformer is called an output transformer and the amplifier is called transformer coupled class A amplifier.*

Before studying the operation of the amplifier, let us revise few concepts regarding the transformer.

8.8.7 Efficiency

The general expression for the efficiency remains same as that given by equations (24) and (25) in section 8.7.

$$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 V_{CC} I_{CQ}} \times 100$$

8.8.8 Maximum Efficiency

Assume maximum swings of both the output voltage and output current, to calculate maximum efficiency, as shown in the Fig. 8.20.

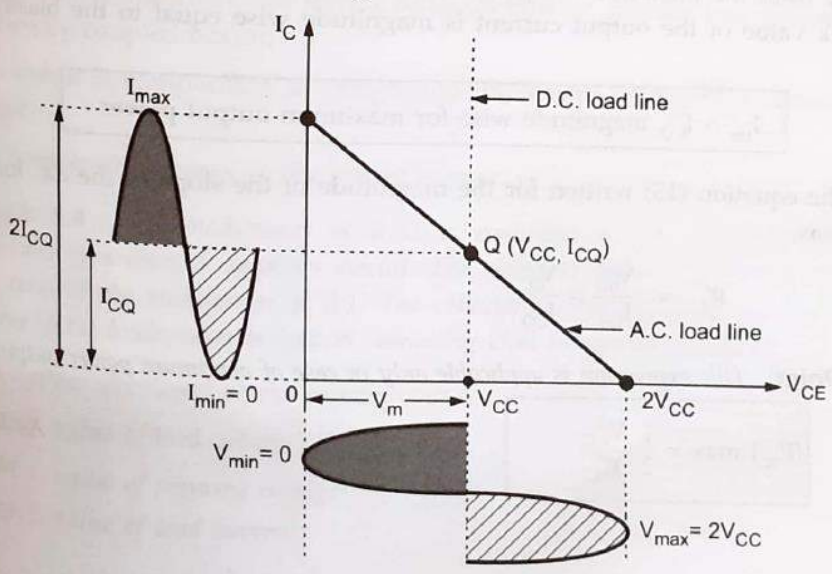


Fig. 8.20 Maximum voltage and current swings

From the Fig. 8.20, assuming that the Q point is exactly at the centre of the load line, for maximum swing we can write,

$$\left.\begin{aligned} V_{min} &= 0 \text{ and } V_{max} = 2\,V_{CC} \\ I_{min} &= 0 \text{ and } I_{max} = 2I_{CQ} \end{aligned}\right\} \text{ for maximum swing}$$

Using equation (25) of section 8.7,

$$\%\,\eta_{max} = \frac{(2V_{CC} - 0)(2I_{CQ} - 0)}{8\,V_{CC}\,I_{CQ}} \times 100$$

$$= \frac{4\,V_{CC}\,I_{CQ}}{8\,V_{CC}\,I_{CQ}} \times 100 = 50\ \%$$

8c. Explain the principle of operation of oscillator and the effect of loop gain on the output of oscillator.

9.3 Barkhausen Criterion

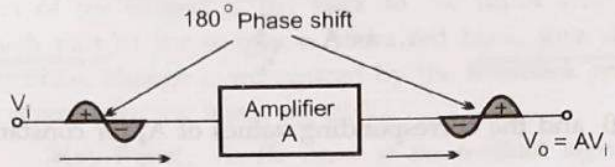


Fig. 9.2 Inverting amplifier

Consider a basic inverting amplifier with an open loop gain A. The feedback network attenuation factor β is less than unity. As basic amplifier is inverting, it produces a phase shift of 180° between input and output as shown in the Fig. 9.2.

Now the input V_i applied to the amplifier is to be derived from its output V_o using feedback network.

But the feedback must be positive i.e. the voltage derived from output using feedback network must be in phase with V_i. Thus the feedback network must introduce a phase shift of 180° while feeding back the voltage from output to input. This ensures positive feedback.

The arrangement is shown in the Fig. 9.3.

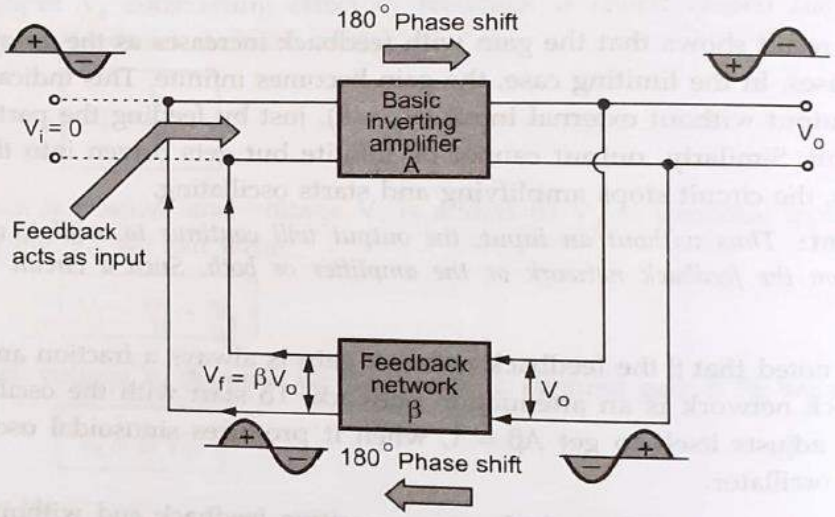


Fig. 9.3 Basic block diagram of oscillator circuit

Consider a fictitious voltage V_i applied at the input of the amplifier. Hence we get,

$$V_o = A\, V_i \quad \ldots(1)$$

The feedback factor β decides the feedback to be given to input,

$$V_f = \beta\, V_o \quad \ldots(2)$$

Substituting (1) into (2) we get,

$$V_f = A\, \beta\, V_i \quad \ldots(3)$$

For the oscillator, we want that feedback should drive the amplifier and hence V_f must act as V_i. From equation (3) we can write that, V_f is sufficient to act as V_i when,

$$|\, A\beta \,| = 1 \quad \ldots(4)$$

And the phase of V_f is same as V_i i.e. feedback network should introduce 180° phase shift in addition to 180° phase shift introduced by inverting amplifier. This ensures positive feedback. So total phase shift around a loop is 360°.

In this condition, V_f drives the circuit and without external input circuit works as an oscillator.

The two conditions discussed above, required to work the circuit as an oscillator are called **Barkhausen Criterion** for oscillation.

9a. With the help of neat diagram, explain the working and characteristics of N- channel JFET.

10.1.1 Characteristics Parameters of JFET

The important characteristics parameters of JFET are as follows :

- Transconductance (g_m)
- Input resistance and capacitance
- Drain to source resistance (r_d)
- Amplification factor (μ)
- Power Dissipation (P_D)

10.1.1.1 Transconductance

The transconductance, g_m, is the change in the drain current for given change in gate to source voltage with the drain to source voltage constant as shown in Fig. 10.3.

Looking at Fig. 10.3, we can say that it is the slope of the transfer characteristic. Since the slope varies, g_m also varies. g_m has a greater value near the top of the curve than it does near the bottom. The transconductance g_m is defined as

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}\ \text{constant}} \quad \ldots(1)$$

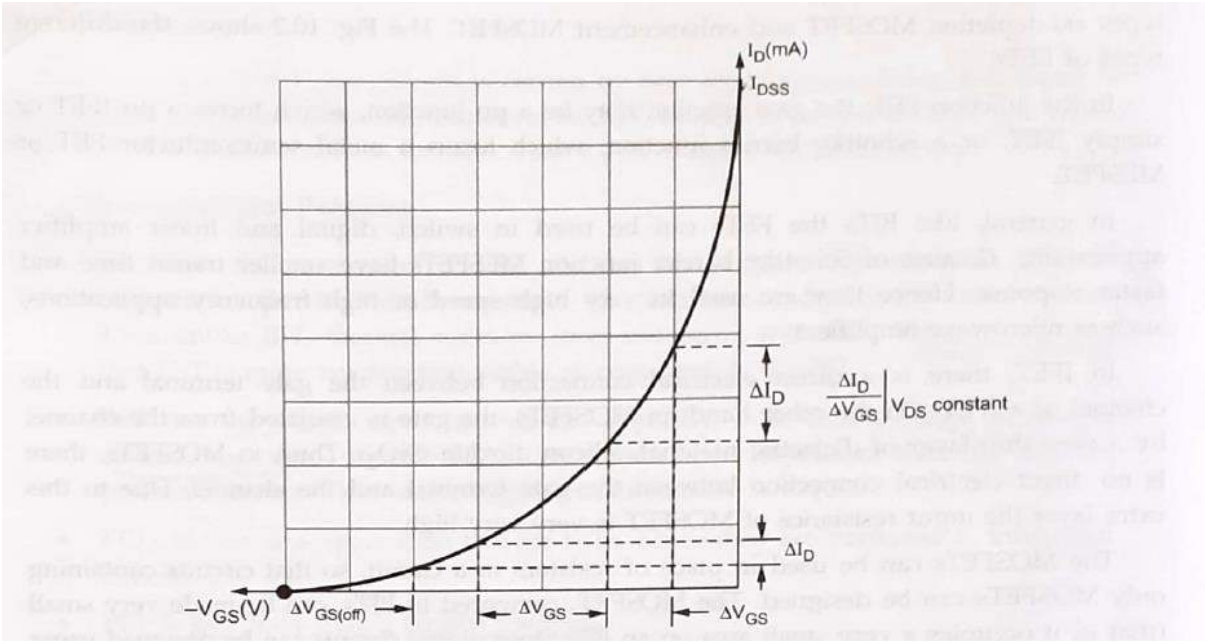


Fig. 10.3 Transconductance g_m varies depending on the bias point (V_{GS})

The transconductance g_m is also called **mutual conductance.** The practical unit for g_m is mS (millisiemen) or mA/V. For given g_m, we can calculate an approximate value for g_m at any point on the transfer characteristic curve using the following equation

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right] \quad \ldots (2)$$

where g_{mo} is the value of g_m for $V_{GS} = 0$, and is given by,

$$g_{mo} = \frac{-2\,I_{DSS}}{V_p} \quad \ldots (3)$$

This can be proved as given below. We know that,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2 \quad \ldots(3a)$$

Differentiating this equation with respect to V_{GS} we get,

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{-2\,I_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_p}\right]$$

$$= g_{mo}\left[1 - \frac{V_{GS}}{V_p}\right] \qquad \text{where} \quad g_{mo} = \frac{-2\,I_{DSS}}{V_p}$$

9b. Determine Zi, Zo and Av for JFET common source amplifier with fixed bias configuration using AC equivalent circuit.

10.7 Common Source (CS) Configuration

In common source amplifier circuit input is applied between gate and source and output is taken from drain and source. In the following sections we see the low frequency equivalent circuits for common source configuration with different biasing techniques.

10.7.1 JFET with Fixed Bias

Fig. 10.48 shows common source amplifier with fixed bias. The coupling capacitor C_1 and C_2 which are used to isolate the dc biasing from the applied ac signal act as short circuits for the ac analysis.

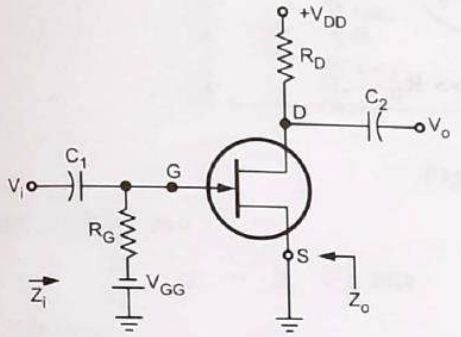


Fig. 10.48 Common source JFET amplifier with fixed bias

Fig. 10.48 shows the low frequency equivalent model for the common source amplifier circuit with fixed bias. It is drawn by replacing :

- All capacitors and dc supply voltages with short circuits and
- JFET with its low frequency equivalent circuit.

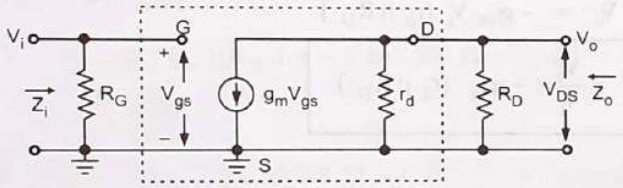


Fig. 10.49 AC equivalent model for the common source amplifier circuit with fixed bias

Now, we see the input impedance output impedance and voltage gain of the above model.

Input impedance Z_i :

Looking into Fig. 10.48 we can say that,

$$Z_i = R_G \qquad \ldots (1)$$

Output Impedance Z_o :

The output impedance Z_o is the impedance measured looking from the output side with input voltage (V_i) equal to 0. As $V_i = 0$,

$V_{gs} = 0$ and hence $g_m V_{gs} = 0$.

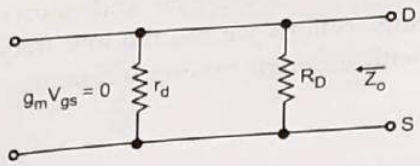


Fig. 10.50

The $g_m V_{gs} = 0$ allows current source to be replaced by an open circuit, as shown in the Fig. 10.49. Therefore the output impedance is

$$Z_o = R_D \,||\, r_d \quad \ldots (2)$$

If the resistance r_d is sufficiently large compared to R_D, then we say that the output impedance is approximately equal to R_D.

$$Z_o \approx R_D \quad \because\ r_d >> R_D \quad \ldots (3)$$

Voltage Gain A_v :

The voltage gain $A_v = \dfrac{V_{ds}}{V_{gs}} = \dfrac{V_o}{V_i}$

Looking at Fig. 10.48 we can write

$$V_o = -g_m V_{gs} \ (r_d \,||\, R_D) \quad \ldots (4)$$

As we know $V_i = V_{gs}$ we can write

$$V_o = -g_m V_i \ (r_d \,||\, R_D) \quad \ldots (5)$$

$$\therefore \quad A_v = \frac{V_o}{V_i} = -g_m \ (r_d \,||\, R_D) \quad \ldots (6)$$

and if $r_d >> R_D$,

$$A_v \approx -g_m R_D \quad \ldots (7)$$

indicates there is a phase shift

9c. Write down the differences between BJT and JFET.

6	Input resistance	Less compare to JFET.	High compare to BJT.
7	Size	Bigger than JFET.	Smaller in construction than BJT, thus making them useful in integrated - circuits (IC).
8	Sensitivity	Higher sensitivity to changes in the applied signals.	Less sensitivity to changes in the applied voltage.
9	Thermal stability	Less	More
10	Thermal runaway	Exists in BJT, because of cumulative effect of increase in I_C with temperature, resulting increase in temperature in the device.	Does not exist in JFET, because drain resistance r_d increases with temperature, which reduces I_D, reducing the I_D and hence the temperature of the device.
11	Relation between input and output	Linear	Non-linear
12	Ratio of o/p to i/p	$\frac{\Delta I_C}{\Delta I_B} = \beta$	$\frac{\Delta I_D}{\Delta V_{GS}} = g_m$
13	Thermal noise	More in BJT as more charge carriers cross junctions.	Much lower in JFET as very few charge carriers cross the junction.
14	Gain bandwidth product	High	Low

10a. With the help of neat diagram, explain the construction, working and characteristics of N-channel depletion type MOSFET.

10.3.1 Depletion MOSFET (D-MOSFET)

10.3.1.1 Construction of n-channel MOSFET

The Fig. 10.22 shows the basic construction of n-channel depletion type MOSFET. Two highly doped n regions are diffused into a lightly doped p type substrate. These two highly doped n regions represent source and drain. In some cases substrate is internally connected to the source terminal.

The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in the Fig. 10.22. The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin layer of dielectric material, silicon dioxide (SiO_2). Thus, there is no direct electrical connection between the gate terminal and the channel of a MOSFET, increasing the input impedance of the device.

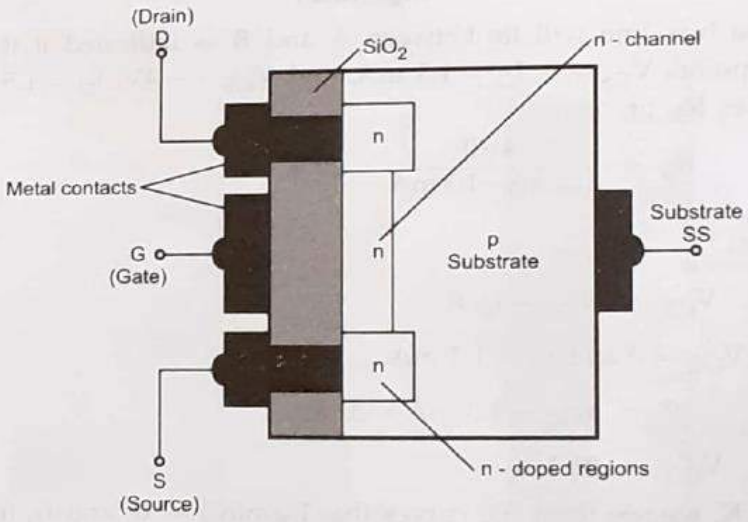


Fig. 10.22 n-channel depletion-type MOSFET

10.3.1.2 Operation, Characteristics and Parameters of n-channel MOSFET

On the application of drain to source voltage, V_{DS} and keeping gate to source voltage to zero by directly connecting gate terminal to the source terminal, free electrons from the n-channel are attracted towards positive potential of drain terminal. This establishes current through the channel to be denoted as I_{DSS} at $V_{GS} = 0$ V, as shown in the Fig. 10.23.

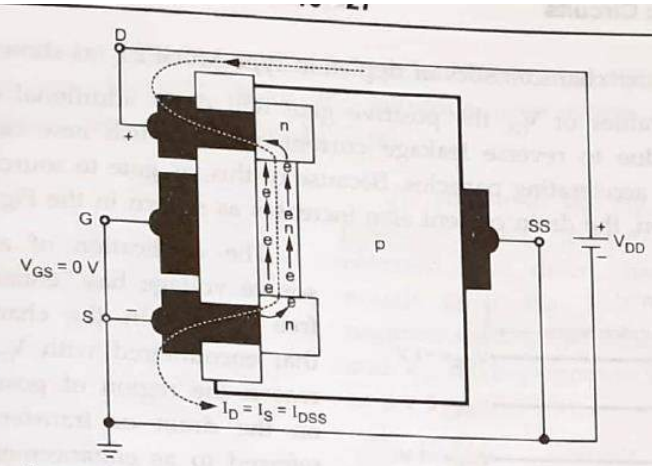


Fig. 10.23 n-channel depletion-type MOSFET with V_{GS} = 0 V and an applied voltage (V_{DD})

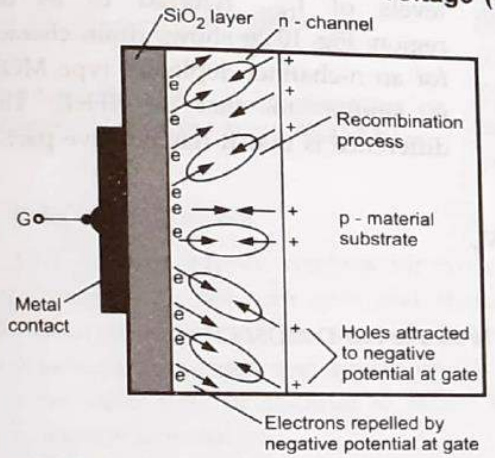


Fig. 10.24 Reduction in free electrons in the n-channel due to negative potential at the gate

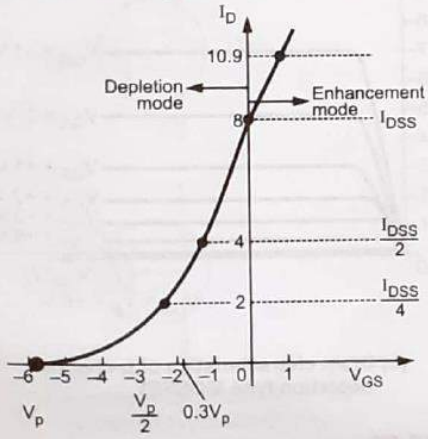


Fig. 10.25 Transfer characteristics for an n-channel depletion type MOSFET

If we apply negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, and attract holes from the p type substrate. This initiates recombination of repelled electrons and attracted holes as shown in the Fig. 10.24.

The level of recombination between electrons and holes depends on the magnitude of the negative voltage applied at the gate. This recombination reduces the number of free electrons in the n-channel for the conduction, reducing the drain current.

In other words we can say that, due to recombinations, n-channel is depleted of some of its electrons, thus decreasing the channel conductivity. The greater the negative voltage applied at the gate, the greater the depletion of n-channel electrons. The level of drain current will reduce with increasing negative bias for V_{GS} as

shown in the transfer characteristics of depletion type MOSFET (as shown in Fig. 10.25).

For positive values of V_{GS} the positive gate will draw additional electrons from the p-type substrate due to reverse leakage current and establish new carriers through the collisions between accelerating particles. Because of this, as gate to source voltage increases in positive direction, the drain current also increases as shown in the Fig. 10.25.

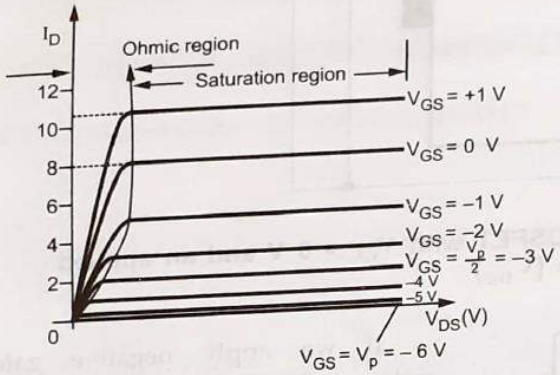


Fig. 10.26 Drain characteristics for an n-channel depletion type MOSFET

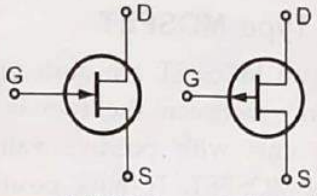
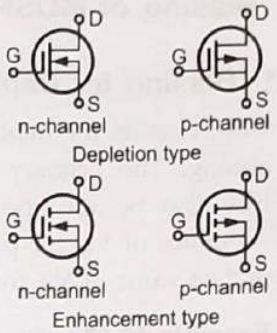
The application of a positive gate to source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with V_{GS} = 0 V. For this reason the region of positive gate voltages on the drain or transfer characteristics is referred to as enhancement region and the region between cut-off and the saturation levels of I_{DSS} referred to as depletion region. Fig. 10.26 shows drain characteristics for an n-channel depletion type MOSFET. It is similar to that of JFET. The only difference is that it has positive part of V_{GS}.

9b. Write down the differences between MOSFET and JFET.

10.3.2.4 Comparison

Comparison of JFET and MOSFET

Sr. No.	Parameter	JFET	MOSFET
1.	Types	a) n-channel b) p-channel	A) n-channel depletion type MOSFET B) p-channel depletion type MOSFET C) n-channel enhancement type MOSFET D) p-channel enhancement type MOSFET

2.	Symbols		
3.	Operation mode	Operated in depletion mode.	Operated in depletion and enhancement mode.
4.	Input impedance	High (> 10 MΩ)	Very high (> 10,000 MΩ)
5.	Gate	Gate is not insulated from channel	Gate is insulated from channel by a layer of SiO_2.
6.	Channel	Channel exists permanently.	Channel exists permanently in depletion type MOSFET, but not in enhancement type MOSFET.

c. For the circuit given in the Fig Q10(c), determine: i) Input impedance ii) Output impedance and iii) voltage gain. **(10 Marks)**

(04 Marks)

(06 Marks)

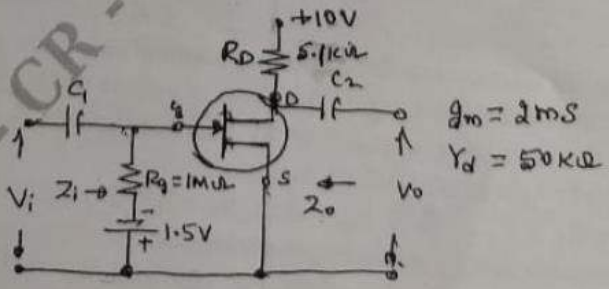


Fig Q10(c)

* * *2 of 2 * *

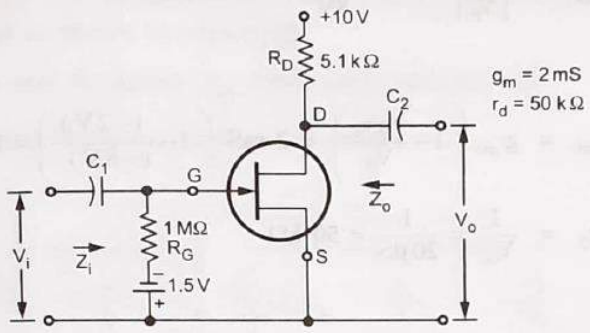


Fig. 10.51

Solution : i) We have

$$Z_i = R_G = \mathbf{1\ M\Omega}$$

ii) We have

$$Z_o = r_d \,||\, R_D = 50\ K \,||\, 5.1\ K = \mathbf{4628\ \Omega}$$

iii) Voltage Gain A_v : We have

$$A_v = -g_m\,(r_d \,||\, R_D) = -2\ mS\ (50\ K \,||\, 5.1\ K) = -2\ mS\ (4628)$$

$$= \mathbf{-9.256}$$