CBCS SCHEME

USN | | | | | | | | | | 18CS33

Third Semester B.E. Degree Examination, Aug./Sept.2020
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With a neat diagram, explain the working principle of photocoupler. **(08 Marks)**

b. List the different types of BJT biasing. Derive the expression for collector emitter voltage (V_{CE}) for fixed bias circuit. **(08 Marks)**

c. Write a note on light emitting diode. **(04 Marks)**

OR

2 a. Explain with neat diagram, the construction, working principle and characteristics equation of photodiode. **(08 Marks)**

b. With a neat waveform and circuit diagram, explain the working of monostable multivibrator. **(06 Marks)**

c. Explain with neat diagram R-2R ladder type DAC and derive the expression for V_0. **(06 Marks)**

Module-2

3 a. Minimize the following function for SOP using K-map and implement it using basic gates: $f(a,b,c,d) = \Pi M(5,7,13,14,15) + d(1,2,3,9)$ **(06 Marks)**

b. Design the function EX-OR using (i) NAND gates only (ii) NOR gates only **(06 Marks)**

c. A switching circuit has two control inputs (C_1 and C_2), two data inputs (X_1 and X_2) and one output Z. The circuit performs one of the logic functions such as OR, XOR, AND, EQU for control inputs combination C_1, C_2 as 00, 01, 10, 11 respectively:

(i) Derive the truth table for Z

(ii) Use a K-map to find minimum AND-OR gate circuit to realize Z. **(04 Marks)**

OR

4 a. Minimize the following function for POS using Kmap and realize it by using basic gates: $f(a,b,c,d) = \Pi M(0,1,6,8,11,12) + d(3,7,4,15)$ **(06 Marks)**

b. Plot the following function on a K-map (Do not expand to minterm before plotting): $F(A,B,C,D) = \overline{A}\,\overline{B} + C\overline{D} + ABC + \overline{A}\,\overline{B}C\overline{D} + AB\overline{C}\overline{D}$, find the minimum sum of products. **(06 Marks)**

c. A digital system is to be designed in which the month of the year is given as I/P is four bit form. The month January is represented as '0000', February as '0001' and so on. The output of the system should be '1' corresponding to the input of the month containing 31 days or otherwise it is '0'. Consider the excess number in the I/P beyond '1011' as don't care condition:

(i) Write truth table, SOP Σm and POSΠM form

(ii) Simplify for SOP using K-map

(iii) Realize using basic gates **(08 Marks)**

Module-3

5 a. Explain with neat diagram static hazard 0 and its recover method. (06 Marks)

b. Implement the following function using $3 \times 4 \times 2$ PLA:
$A(x,y,z) = \sum m(0,1,3,4)$; $B(x,y,z) = \sum m(1,2,3,4,5)$ (08 Marks)

c. Using EVM method simplify the following function and implement it by using 8:1 MUX
$F(a, b, c, d) = \Sigma m(0, 1, 2, 4, 5, 6, 9, 10, 12, 13, 14, 15)$ (06 Marks)

OR

6 a. With a neat diagram, explain 3 to 8 line decoder. (04 Marks)

b. Construct 32:1 MUX using 8:1 MUX and 2:4 decoder. (08 Marks)

c. Design 7 segment decoder and realize using PLA. (08 Marks)

Module-4

7 a. Explain with a neat diagram, VHDL program structure. (06 Marks)

b. Construct SR gates latch using NAND gates and derive the characteristics equation for the same. (08 Marks)

c. Explain T-flipflop with characteristics equation. (06 Marks)

OR

8 a. Explain with neat diagram, working of JK flipflop and derive its characteristic equation. (08 Marks)

b. Write VHDL code for 4 bit adder. (06 Marks)

c. Explain the application of SR latch in switch debouncing technique. (06 Marks)

Module-5

9 a. With neat diagram, explain 4 bit parallel adder with accumulator. (08 Marks)

b. With diagram explain 4 bit SISO register. (08 Marks)

c. Write a note on Johnson tail counter. (04 Marks)

OR

10 a. Design Mod 5 counter using JK flipflops. (10 Marks)

b. Explain 4 bit PIPO shift register with block diagram. (06 Marks)

c. Write a note on ring counter. (04 Marks)

* * * * *