(06 Marks)

hird Semester B.E. Degree Examination, Aug./Sept.2020 **Analog Electronic Circuits**

Time: 3

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- Explain the working of series clipper to clip the input sinusoidal signal: 1 (ii) below V_R. Draw the input and output waveforms and transfer (i) above V_R characteristic. Neglect cut in voltage V_r. Assume clipping action in positive half cycle of
 - input signal. b. Define operating point in a transistor and explain its significance. (04 Marks)
 - c. Explain the dc analysis of emitter stabilized bias circuit, for this circuit if $R_c = 1 \text{ k}\Omega$, $R_B = 220 \text{ k}\Omega$, $R_E = 1 \text{ k}\Omega$, calculate I_B , I_C , I_E V_{CE} and V_B . Assume $\beta = 200$. (10 Marks)

- For collector to base bias circuit obtain expressions for stability factors S_{ICO}, S_{UBE} and S₆.
 - b. Design a voltage divider bias circuit if $V_{CC} = 12V$, $V_{CE} = 6V$, $V_{E} = 1V$, $I_{C} = 1$ mA, $S_{ICO} = 20$, (10 Marks) $\beta = 100$. Draw the circuit

Module-2

- Develop h-parameter model for transistor amplifier, hence draw h-parameter model for CB, CE and CC modes.
 - b. For a single stage CE amplifier, $R_s = 1 \text{ k}\Omega$, $R_1 = 50 \text{ k}\Omega$, $R_2 = 2 \text{ k}\Omega$, $R_c = 2 \text{ k}\Omega$, $R_L = 2 \text{ k}\Omega$, $h_{ie} = 50$, $h_{oe} = 25 \mu A/V$, $h_{ie} = 1.1 k\Omega$ and $h_{re} = 2.5 \times 10^{-4}$. Calculate A_V, R_i, A_i, A_{IS}, A_{VS} and R₀. Draw the circuit diagram. Use approximate hybrid model. Across RE, bypass capacitor (10 Marks) is used.

OR

- For common emitter amplifier with collector to base bias circuit, determine A_I, Z_i, A_v, A_{vs}, A_{IS} and Z'_{0} . Draw circuit diagram. $R_{B}=200~k\Omega$, $R_{c}=10~k\Omega$, $h_{ie}=1.1~k\Omega$, $h_{fe}=50$, $h_{oe} = h_{re} = 0$ and $R_s = 1 k\Omega$. (10 Marks)
 - b. For emitter voltage follower circuit, obtain expression for A_I , Z_i , A_V , R_0 and R_0 . Use approximate hybrid model. Also state features of emitter follower circuit. (10 Marks)

Module-3

- For the Darlington connection, obtain expression for A_{I2} , R_{i2} for II stage and A_{I1} , R_{i1} for (10 Marks)
 - b. Consider a 2 stage RC coupled amplifier for the I stage $R_S = 1 \text{ k}\Omega$, $R_{Ci} = 15 \text{ k}\Omega$, $R_{Ei} = 100 \Omega$ $R_1 = 200 \text{ k}\Omega$, $R_2 = 20 \text{ k}\Omega$. For II stage $R_{C2} = 4 \text{ k}\Omega$, $R_{E2} = 330 \Omega$, biasing resistors R_3 = 47 k Ω , R_4 = 4.7 k Ω . Bypass capacitor is connected across R_{E_1} and R_{E_2} . Assume $h_{ie} = 1.2 \text{ k}\Omega$, $h_{fe} = 50$, $h_{oe} = 25 \mu\text{A/V}$, $h_{re} = 2.5 \times 10^{-4}$, Determine the overall A_V, A_{VS}, R₀₁' and Ro2'. Draw the circuit diagram. (10 Marks)

OR

- 6 a. Explain the concept of voltage amplifier, current amplifier, transconductance amplifier and transresistance amplifier using Thevenin's or Norton's equivalent circuit. (10 Marks)
 - b. For voltage shunt feedback amplifier topology, obtain expressions for R_{if} and R_{of}.

(10 Marks)

Module-4

- 7 a. Obtain an expression for 2nd harmonic distortion in a power amplifier using 3-point method.

 (10 Marks)
 - b. A class-B push pull amplifier supplies power to a resistive load of 12 Ω . The turns ratio of output transformer is 3:1 and $\eta = 78.5\%$. Determine the maximum power output, maximum power dissipation in each transistor maximum base and collector current in each transistor. Assume $V_{cc} = 20 \text{ V}$ and $h_{fe} = 25$. (10 Marks)

OR

- 8 a. Obtain expression for f_0 and h_{fe} in Colpitt's RF oscillator. (10 Marks)
 - . Compare RC phase shift and Wein bridge oscillator. (05 Marks)
 - c. Calculate the values of R and C in a RC phase shift oscillator if $f_0 = 500$ Hz. Draw the circuit diagram. Assume $C = 0.1 \mu F$. (05 Marks)

Module-5

- 9 a. Explain construction, operation and characteristics of enhancement MOSFET. (10 Marks)
 - b. Compare D-MOSFET and E-MOSFET. (05 Marks)
 - c. Define transconductance " g_m " in FET and Show that $g_m = g_{m_o} \left(1 \frac{V_{GS}}{V_p} \right)$ (05 Marks)

OR

- 10 a. Consider voltage divider bias circuit of JFET. If $R_D=1.2~k\Omega$, $R_S=2~k\Omega$, $R_1=20~k\Omega$, $R_2=10~k\Omega$, $V_{DD}=12V$, $I_{DSS}=12~mA$, $V_P=-4V$, calculate I_D , V_{GS} , V_G , V_{DS} and V_S . Draw the circuit diagram. (10 Marks)
 - b. Consider JFET in fixed bias mode. Derive expressions for Z_{in} , Z_0 and A_V . If $R_G=1$ M Ω , $r_d=50$ k Ω , $g_m=2$ m s , calculate Z_i , A_v and Z_0 . Draw the circuit diagram $R_D=5.1$ k Ω .

(10 Marks)

