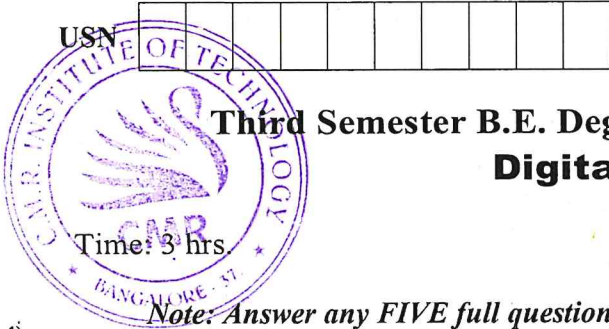


# CBCS SCHEME

15EC33



## Third Semester B.E. Degree Examination, Aug./Sept.2020 Digital Electronics

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

### Module-1

- 1 a. i) Convert the following expression in standard SOP and also represent in decimal notation form  $f(A, B, C) = AC + BC + AB$   
ii) Convert the following expression in standard POS form and also represent in decimal notation  $f(A, B, C) = (A + B)(B + C)(A + C)$  (08 Marks)  
b. Reduce the following using K-map and draw the logic diagram using NAND gates for the reduced expression:  $f(a, b, c, d) = \sum m(6, 7, 9, 10, 13) + dc(1, 4, 5, 11, 15)$  (08 Marks)

OR

- 2 a. Reduce the following function using K-map technique and Implement using NOR-gates  $f(a, b, c, d) = \pi M(0, 3, 4, 7, 8, 10, 12, 14) + dc(2, 6)$  (06 Marks)  
b. Simplify the following using Quine-Mc Cluskey method and draw the logic diagram using NAND gates for the reduced expression:  
 $f(w, x, y, z) = \sum m(1, 2, 3, 5, 9, 12, 14, 15) + \sum dc(4, 8, 11)$  (10 Marks)

### Module-2

- 3 a. Write and explain 2 to 4 decoder. (06 Marks)  
b. Implement the following functions using ICS 74 x 138  
 $f_1(a, b, c, d) = \sum m(0, 4, 8, 10, 14, 15)$   
 $f_2(a, b, c, d) = \sum m(3, 7, 9, 13)$  (10 Marks)

OR

- 4 a. Implement the following Boolean function with 8:1 MUX  
 $F(A, B, C, D) = \sum m(0, 2, 6, 10, 11, 12, 13) + dc(3, 8, 14)$  (08 Marks)  
b. Explain the look ahead carry generator. (08 Marks)

### Module-3

- 5 a. Write and explain JK Flip-Flop by Truth table and logic diagram. (06 Marks)  
b. Write the excitation table of JK Flip-Flop. (04 Marks)  
c. Write the characteristic equation of SR Flip-Flop. (06 Marks)

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OR

- 6 a. Explain the Master-slave JKFF with logic diagram and truth table. (10 Marks)  
b. Explain the Negative Edge triggered JK Flip-Flop. (06 Marks)

### Module-4

- 7 a. Write and explain parallel in serial out shift register by writing logic diagram and timing diagram. (10 Marks)  
b. Write and explain 3-bit asynchronous counter. (06 Marks)

OR

- 8 a. Design a mod-6 synchronous counter using JK Flip-Flop. (10 Marks)
- b. Write and explain counter applications. (06 Marks)

**Module-5**

- 9 a. Write the difference between Moore model and Mealy model. (06 Marks)
- b. Design a mealy type sequence detector to detect a serial input sequence of 101. (10 Marks)

OR

- 10 a. Design a clocked sequence circuit that operates according to the state diagram shown in Fig.Q.10(a). Implement the circuit using D-Flip-Flop.

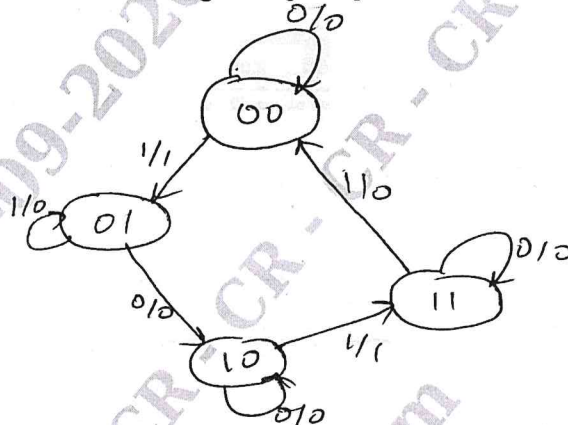


Fig.Q.10(a) State diagram

(08 Marks)

- b. Obtain the transition table for the given state diagram shown in Fig.Q.10(b) and design the sequential network using JK Flip-Flop.

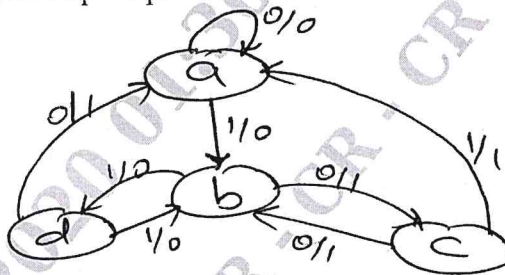


Fig.Q.10(b) State diagram

(08 Marks)

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